LOW DISTORTION
TRANSISTOR POWER AMPLIFIERS

JAMES N. JAMESON

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LOW DISTORTION TRANSISTOR

POWER AMPLIFIERS

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POWER AMPLIFIERS

by

James Nicholas Jameson

Lieutenant, United States Navy

Submitted in partial fulfillment
of the requirements
for the degree of
MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

United States Naval Postgraduate School
Monterey, California

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Thesis
[illegible]

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the thesis requirements for the degree of

MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

from the
United States Naval Postgraduate School

PREFACE

This paper shall deal primarily with a three stage transistor power amplifier employing two germanium rate grown junction transistors and one silicon rate grown junction transistor, the latter serving as the final amplifier stage.

It is the aim of this paper to point out the problems encountered in the design of such an amplifier and the approaches used by the writer in solving these problems.

Considerable emphasis shall be placed on the subject of distortion and the means taken to provide for its minimization.

The work performed in the development of this amplifier was done at the Lenkurt Electric Company at San Carlos, California.

The writer wishes to express his gratitude to Professor A. Sheingold for his sincere interest, guidance, and assistance in the preparation of this paper. The writer also wishes to gratefully acknowledge the assistance of Mr. B. R. Stack of the Lenkurt Electric Company in the development of this amplifier.

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TABLE OF SYMBOLS AND ABBREVIATIONS

(Listed in the order of their use in the text)

a - Current amplification factor

r_b - Equivalent base resistance

r_c - Equivalent collector resistance

r_e - Equivalent emitter resistance

r_m - Equivalent emitter-collector transresistance

r_l - A-C load resistance

P_G - Low frequency power gain

I_{co} - D-C collector current for zero emitter current

S - Stability factor

V_c - D-c collector voltage

I_c - D-c collector current

f_{aco} - Frequency at which /a/ is reduced by 3db

f_{bco} - Frequency at which /b/ is reduced by 3 db

b - Grounded emitter current amplification factor

CHAPTER I

INTRODUCTION

1. General.

Since its discovery in 1948 the role of the transistor has changed from one of a mysterious laboratory curiosity with relatively little practical value to one of great potential in numerous applications in electronic circuitry.

Though originally a low power device, in recent years the trend of the power handling capacity of the transistor has been steadily upward.

Among recent achievements are the building of a number of transistors capable of handling power up to 40 watts, and production of transistors handling power of the order of 100 milliwatts. In the development stage are transistors with power dissipation ratings of two or three watts. [14]

With these advancements being made in the fabrication of the transistor, the use of this device in the capacity of a power amplifier is showing considerable promise.

2. The Transistor Power Amplifier.

In designing the transistor power amplifier a different approach must be used than that taken when designing a vacuum tube power amplifier. This is due primarily to the limitation of maximum available transistor power gain to about 40 db. Therefore, unlike vacuum tubes where power amplification is left almost entirely to the final stage of an amplifier, in the transistor amplifier each stage contributes power gain. Each stage must, therefore, be designed independently for

power gain with the basic design consideration being controlled by the overall demands of the amplifier. These demands are many. The most important are power output, power gain, frequency response, and distortion.

3. Summary.

This thesis shall deal primarily with a transistor power amplifier to be used in a carrier telephone system by the Lenkurt Electric Company. The needs of the system require that the below listed specifications be met by the amplifier: (1) Gain - 40 db, (2) frequency response - ± .25 db from 40 to 80 kilocycles, (3) power output - 13 dbm, (4) distortion - down 43 db at 10 dbm power output, (5) input and output impedances - 600 ohms ± 15%, (6) use no more than 3 transistors.

CHAPTER II

FINAL AMPLIFIER

1. General.

The final stage of the transistor power amplifier presents the most challenging problem. The power output requirements of this stage are high and considerable precautions must be taken to keep the distortion within the specifications of the amplifier. Because of the stringent distortion requirements, this stage is limited to either the single ended class A grounded base configuration or a push pull grounded base arrangement. Push pull operation results in cancellation of the even harmonics and at first glance would seem to be preferable to the single ended connection. This arrangement, however, would require the use of two transistors which must be closely matched in order for the cancellation process to be fully effective. Because of this limitation, the single ended grounded base configuration presents a more realistic solution to the problem at hand.

2. Power Output.

Figure 1. shows the output characteristics for the Texas Instruments silicon transistor Ti-903. Since low distortion is a prime requisite, it is evident that the use of the grounded base configuration is mandatory.

Also shown on figure 1. by the dotted line, is the contour for maximum permissible collector dissipation. It is reasonable to assume that the dissipation in the emitter is negligible since the voltage across the emitter is very small. Hence, the dissipation contour may be considered to represent the total permissible power dissipation for

the transistor.

The shaded areas of figure 1. represent the maximum limits of collector current and collector voltage. The operation of the transistor, therefore, is limited to the area ABCDE. In order to obtain the maximum power output without introducing distortion the points I_{c2} equals 10 ma and V_{c2} equals 30v are considered the end points of the required load line. From these values the optimum load line is

$$\frac{V_{c2} - V_{c1}}{I_{c2} - I_{c1}} = \frac{30 - 1}{10 - .25} = 2.9 \text{ K}$$

and the quiescient operating point is $V_o = V_{c1} + \frac{V_{c2} - V_{c1}}{2} = 15.5$, and $I_o = I_{c1} + \frac{I_{c2} - I_{c1}}{2} = 5$ ma.

The power output is $P_o = \frac{(V_{c2} - V_{c1})\,(I_{c2} - I_{c1})}{8}$

$$= \frac{(30-1)\,(10-.25)}{8} = 35 \text{ mw}$$

The circuit of figure 2 was used to obtain the optimum load experimentally. The results are shown in figure 3. From the data of figure 3 the value of 4K was selected as the optimum load, and to provide an output impedance of 600 ohms the final stage was terminated with an impedance matching transformer.

3. Gain.

Although it is desirable to get as much gain as possible from the final stage, this is not the prime purpose of the stage. It must first develop the required power without exceeding the distortion limitations and secondly provide power gain.

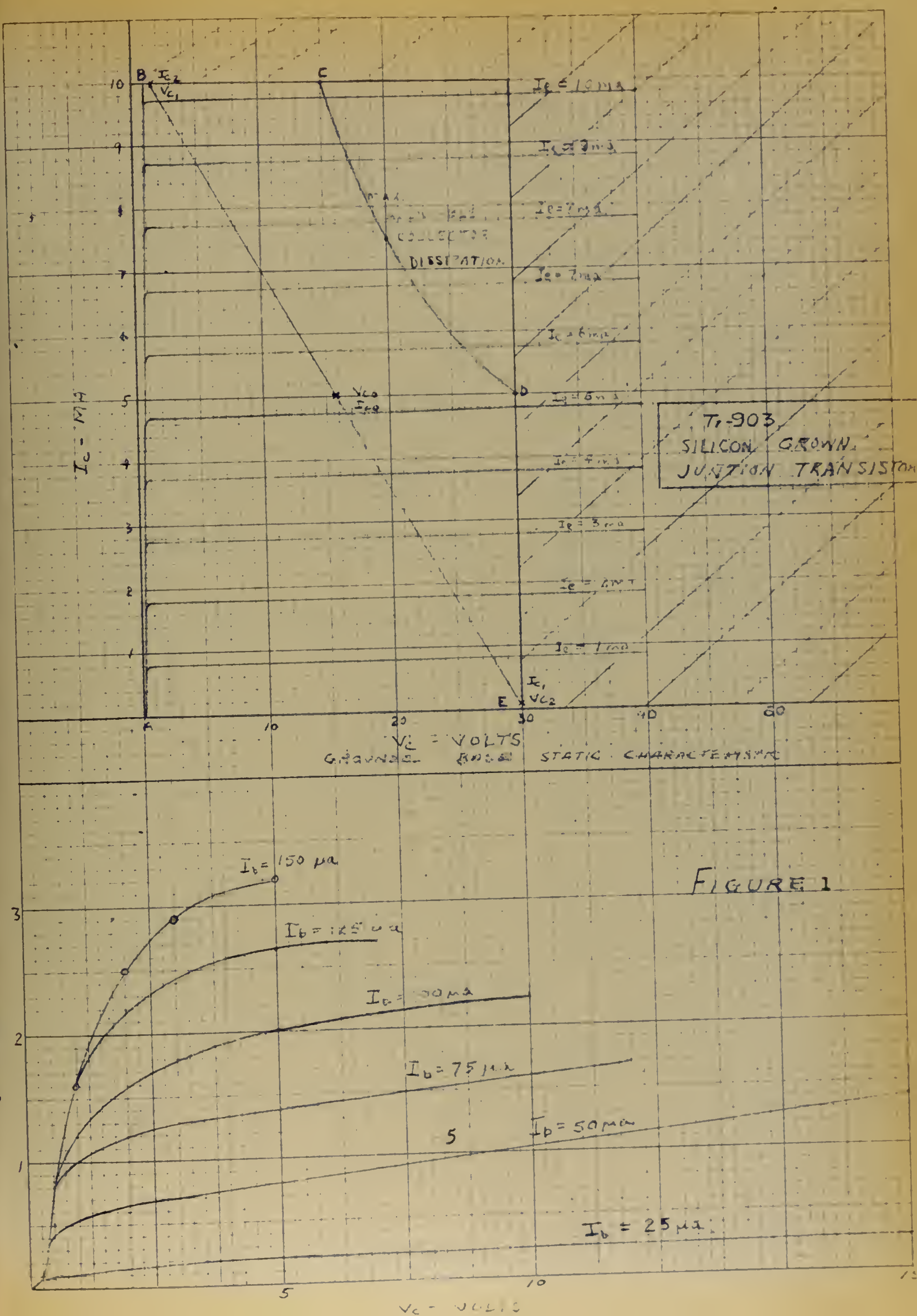
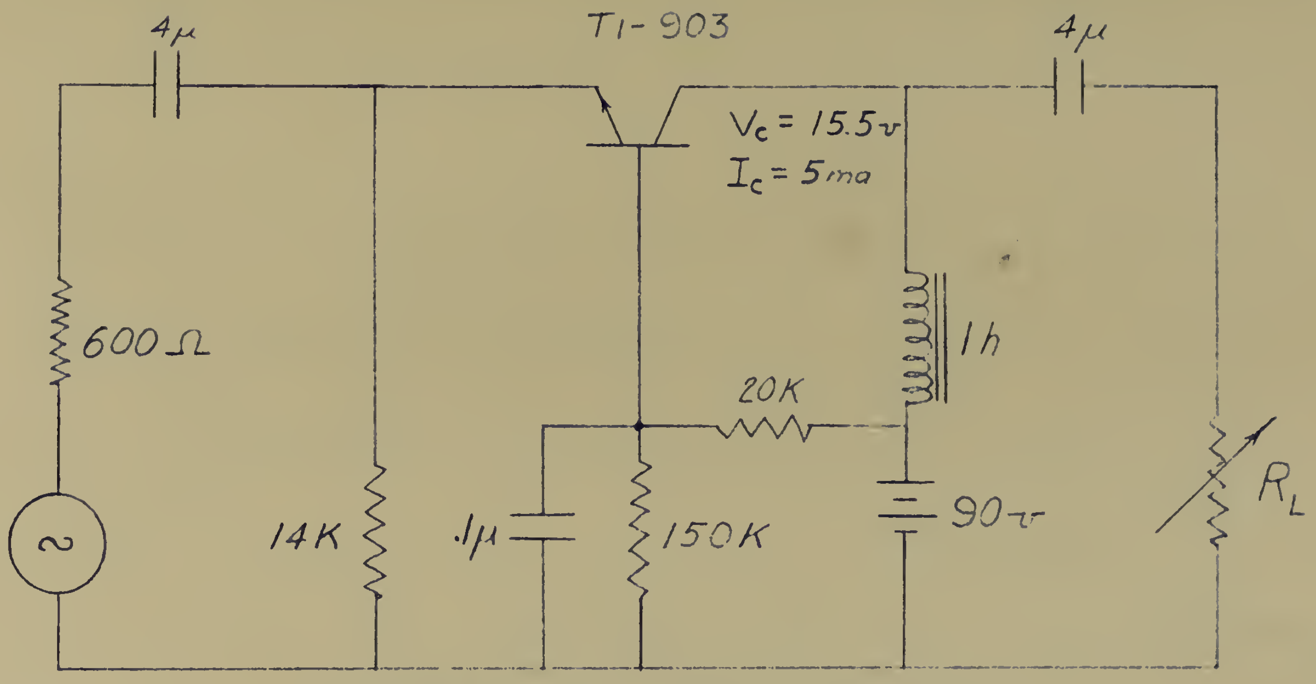
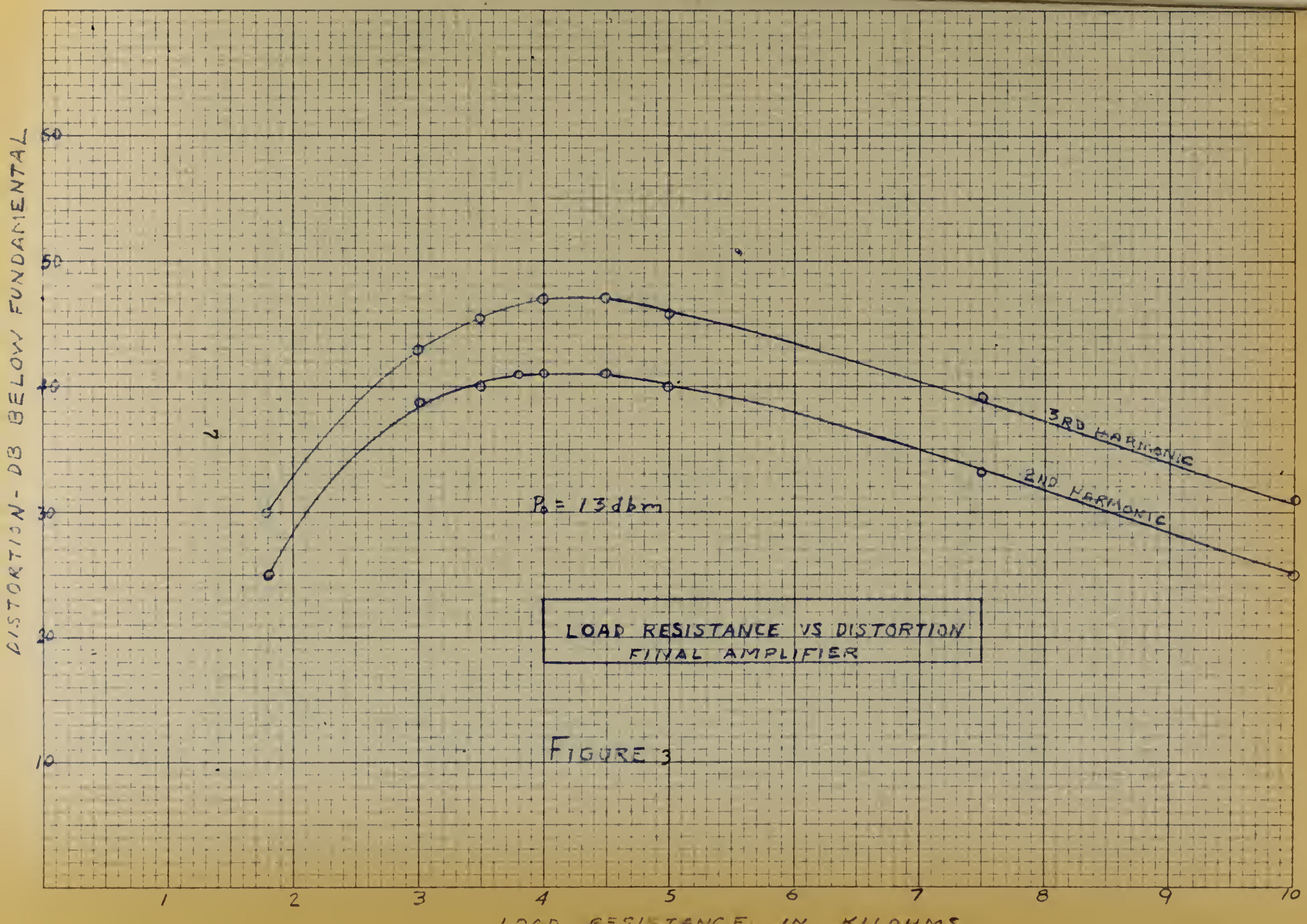
Ti-903
SILICON GROWN
JUNTION TRANSIST
GROUNDED BASE STATIC CHARACTERISTIC
Ic - MA
Vc = VOLTS
B
C
D
E
A
Ic2
Vc1
Vcq
Icq
Ic1
Vc2
MAX. COLLECTOR DISSIPATION
Ie = 10 ma
Ie = 9 ma
Ie = 8 ma
Ie = 7 ma
Ie = 6 ma
Ie = 5 ma
Ie = 4 ma
Ie = 3 ma
Ie = 2 ma
Ie = 1 ma
1
2
3
4
5
6
7
8
9
10
10
20
30
40
50
Ib = 150 μa
Ib = 125 μa
Ib = 100 μa
Ib = 75 μa
Ib = 50 μa
Ib = 25 μa
Ic - ma
Vc - volts
1
2
3
5
10
5

FIGURE 1



GROUNDED BASE AMPLIFIER WITH VARIABLE LOAD

FIGURE 2



LOAD RESISTANCE VS DISTORTION
FINAL AMPLIFIER

FIGURE 3

When operating at frequencies much lower than a_{co} of the transistor, power gain for the grounded base stage may be expressed as:

$$P_G = \frac{(r_m + r_b)^2 \, r_l}{(r_b + r_c + r_l)\left[r_b \, (r_c - r_m + r_e + r_l) + r_e \, (r_c + r_l)\right]} \qquad [10]$$

When $r_e \ll r_c - r_m$; $r_b \ll r_c$; $r_e \ll r_l \ll r_c - r_m$ then power gain may be expressed approximately as

$$P_G = \frac{a^2 \quad r_l}{r_e + r_b \, (1-a)}$$

Using the values of a T1-903 Silicon Transistor

$r_e = 8.7$ ohms

$r_b = 30.8$ ohms

$r_c = 1.025$ M

$a = .93$

$r_l = 4$K

then the power gain of the final stage is

$P_G = 25$ db

4. Bias Stabilization.

It is noted in figure 1. that in order to swing the output from one end of the load line to the other without clipping prematurely it becomes necessary to judiciously select the operating point. Furthermore, it becomes extremely important that this operating point be rigidly stabilized. This is complicated further by the fact that at higher power outputs considerable internal heating results in the transistor. This, in turn, may cause I_{co} to increase to many times

its room temperature value. Unless the bias arrangement is properly designed this variation will produce a departure from the desired operation. The same effect may also be brought about by the changing of transistors, since appreciable variation in parameters among transistors is common.

In order to insure proper stabilization of the operating point, the single battery circuit is employed, as shown in figure 4.

By making the assumptions that (1) V_c, the collector-base voltage, is held within the region where it has a minor effect on the collector current, (2) $a = \left(\frac{\partial I_c}{\partial I_e}\right)_{V_c}$ is constant over the operating range, and (3) V_e, the emitter-base voltage, is zero, the following basic relationships can be stated:

$$I_2 R_2 = I_e R_1 \quad E - I_3 R_3$$

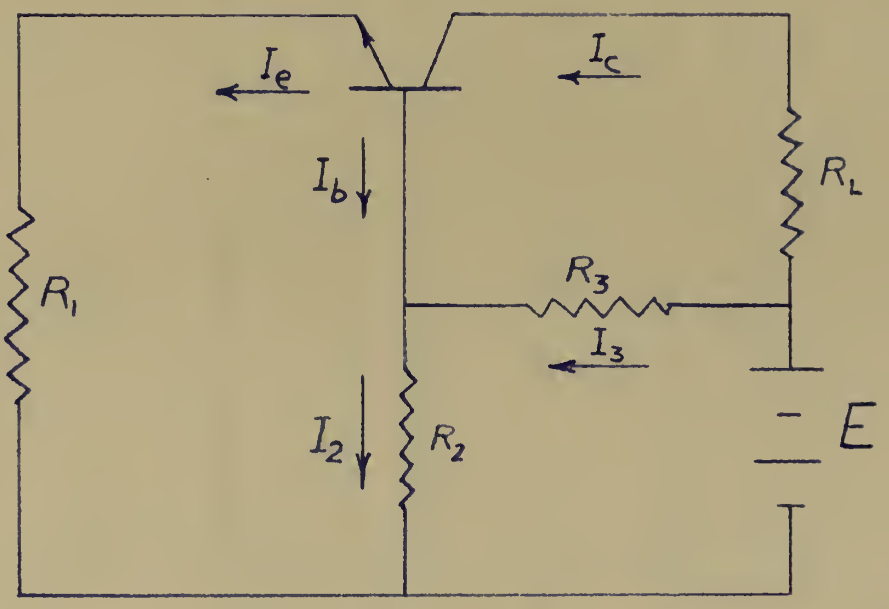
$$I_c = I_b + I_e$$

$$I_b = I_2 - I_3$$

$$I_c = I_{co} + aI_e$$

Defining S, the stability factor, as $\frac{\partial I_c}{\partial I_{co}}$, and solving the above equations

$$R_1 = \frac{-a(E - R_2 I_c - V_c)}{I_c - I_{co}} \qquad [10]$$



SINGLE BATTERY BIAS CONNECTIONS

FIGURE 4

$$R_3 = \frac{E\,(S - 1)}{I_c - SI_{co}}$$

$$R_2 = \frac{R_1\;R_3\quad(S - 1)}{R_3\;\;Sa\;\; - (S - 1)(R_1 + R_3)}$$

The stability factor S means that any change in I_{co} will appear, multiplied S times in the collector current. It is, therefore, desirable to keep S small. Actually, a practical range exists for S below which excessive power is required from the power supply and above which the output current will vary excessively with temperature.

5. Source Impedance.

Before leaving the final amplifier, it becomes necessary to consider the source impedance effects on the circuit. In order to keep the distortion low in this stage the linearity of the input circuit as well as the output circuit of the transistor must be considered. The input distortion may be investigated as follows. The small signal input impedance of a grounded base transistor for any particular load may be approximately stated as

$$r \approx \frac{dE_e}{dI_e} \approx \frac{K_2}{I_e + K_1}$$

where K_1 and K_2 are constants, and E_e and I_e are the emitter voltage and current respectively. For an operating point E_{eo} and I_{eo} and for a sinusoidal input $V_e = v \sin wt$

$$i_e = (I_{eo} + K1)\left[\exp\left(\frac{v \sin wt}{K}\right) - 1\right]$$

Figure 5 [10] shows the effect of increasing the source resistance on the emitter current.

Thus increasing the resistance in the input circuit tends to remove the effect of the non-linearities.

In figure 6 can be seen the effect of varying the source impedance in the final stage.

To keep down the distortion in this stage it becomes necessary to provide some degree of mismatch between the driver stage and the output stage since the input impedance of the stage $\approx$ 20 ohms. This introduces a small power loss. The power available to the amplifier now becomes

$$P_A = P_o \quad \frac{4R_g\ R_l}{(R_g + R_l)^2}$$

where P_A = power available to input of amplifier

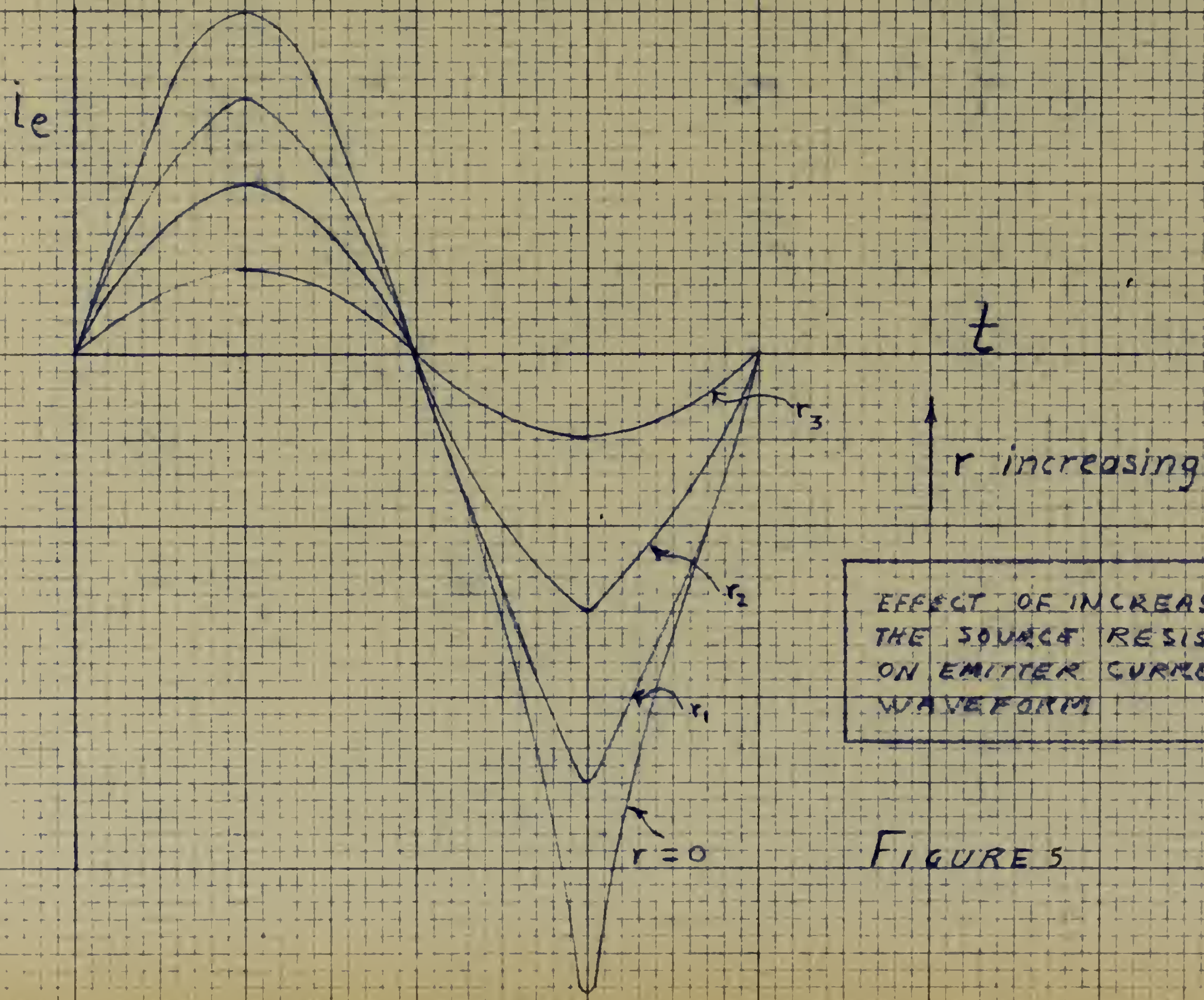
P_o = power available to input of amplifier when input impedance equals the generator impedance

R_g = generator impedance

R_l = load impedance

6. Summary of Final Stage Characteristics.

The complete circuit of the final stage of the power amplifier is shown in figure 7. Figures 7 and 8, are curves representing the performance of the stage with respect to frequency response and distortion.



EFFECT OF INCREASING THE SOURCE RESISTANCE ON EMITTER CURRENT WAVEFORM

FIGURE 5

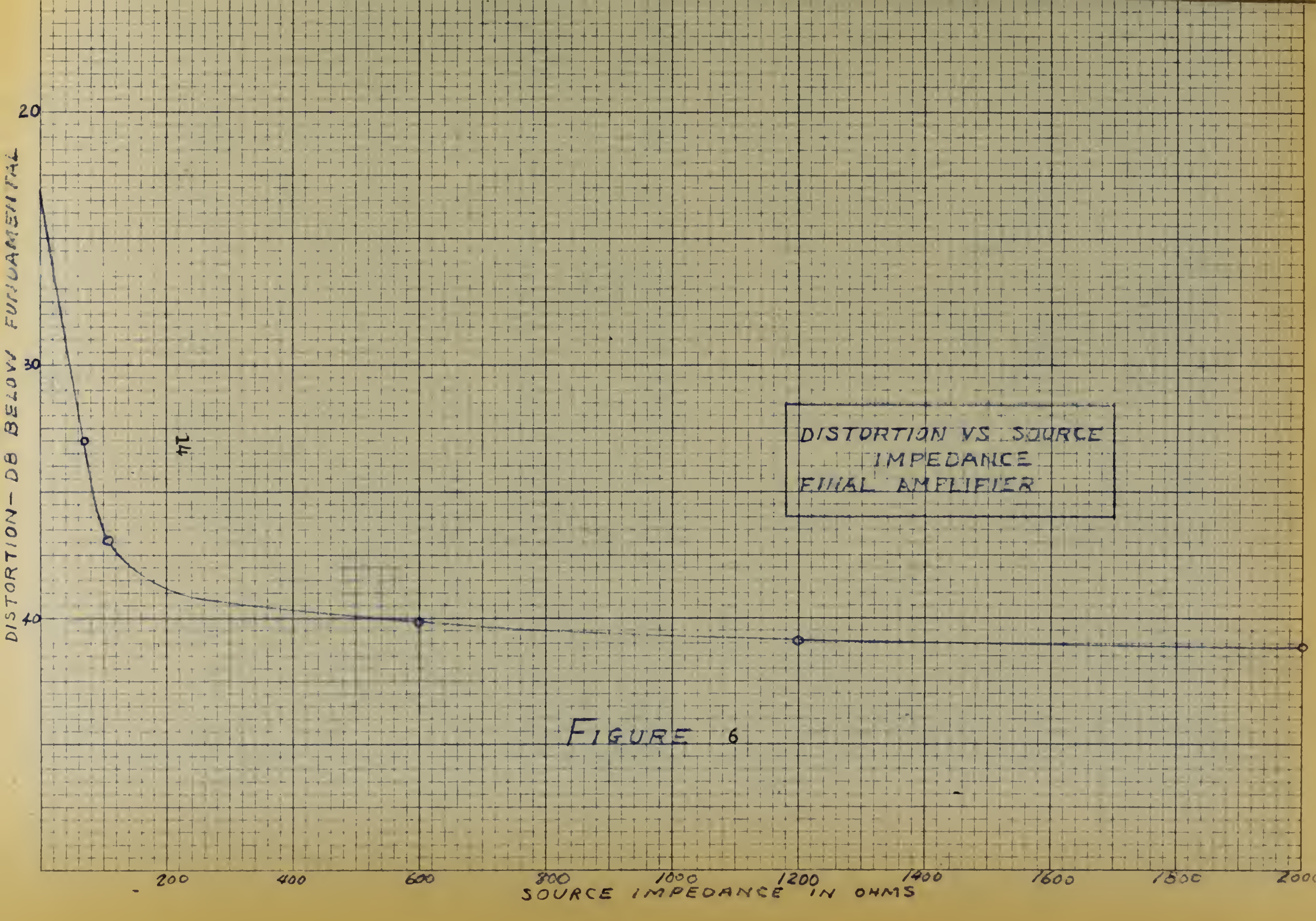

DISTORTION VS SOURCE
IMPEDANCE
FINAL AMPLIFIER
DISTORTION- DB BELOW FUNDAMENTAL
20
30
40
200
400
600
800
1000
1200
1400
1600
1800
2000
SOURCE IMPEDANCE IN OHMS

FIGURE 6

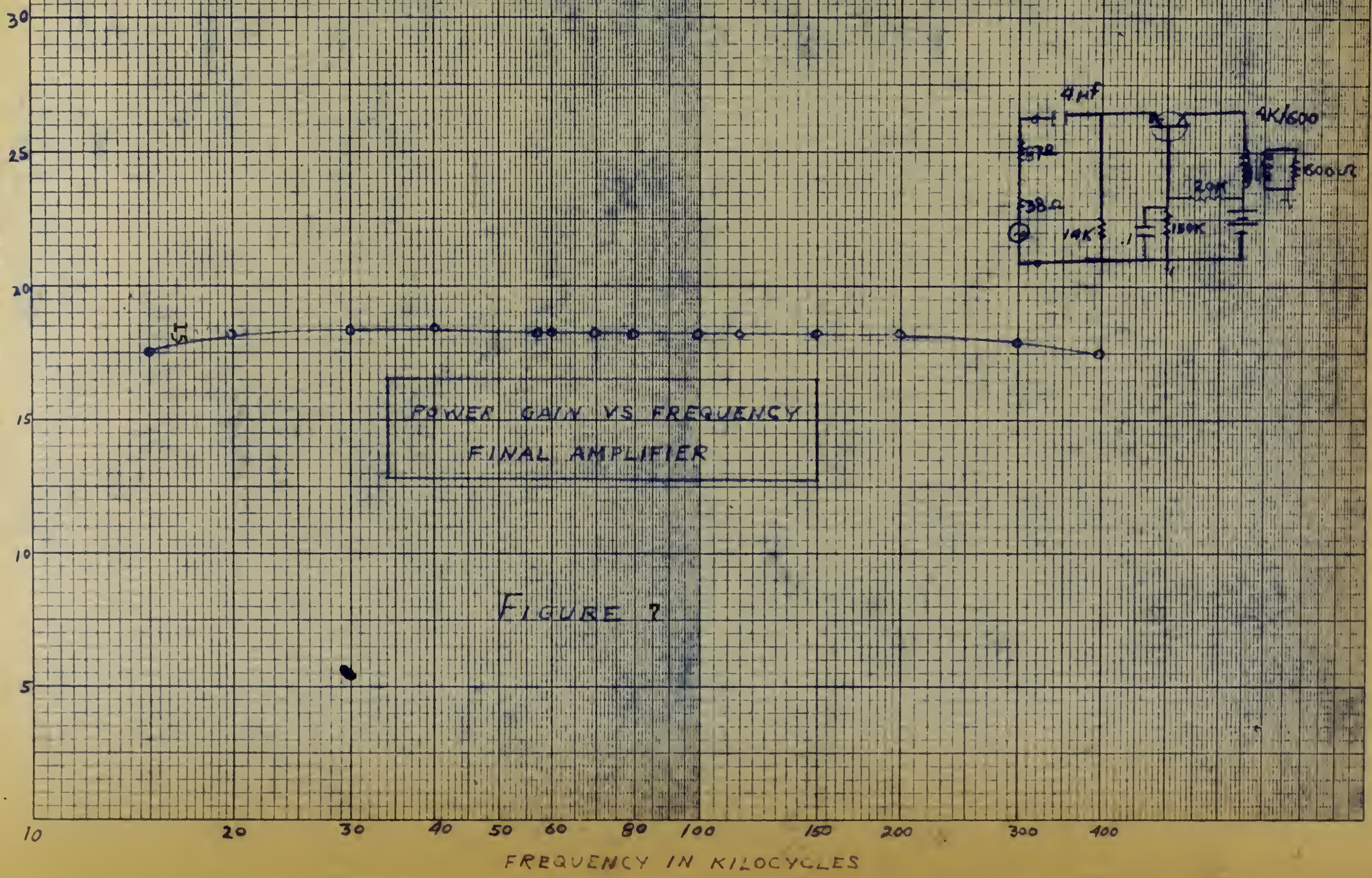

POWER GAIN VS FREQUENCY
FINAL AMPLIFIER
30
25
20
15
10
5
10
20
30
40
50
60
80
100
150
200
300
400
FREQUENCY IN KILOCYCLES
15
4µF
57Ω
38Ω
14K
.1
150K
20K
4K/600
600Ω

FIGURE 7

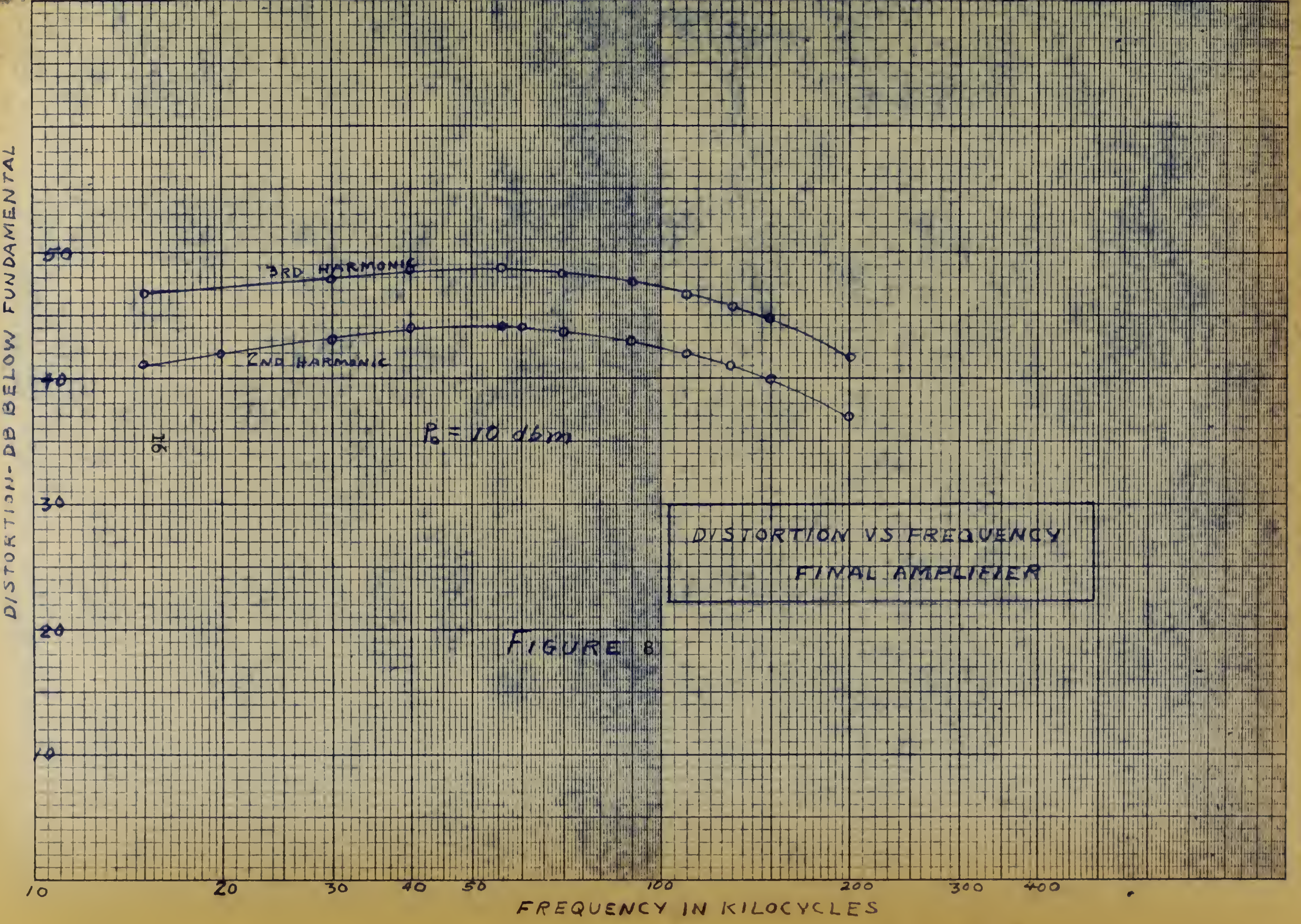


FIGURE 8

DISTORTION VS FREQUENCY
FINAL AMPLIFIER

CHAPTER III

THE DRIVER STAGE

1. General.

Since the driver stage is not required normally to operate at its maximum limits of power output the distortion problem is somewhat reduced, and a certain degree of freedom exists in the selection of the driver stage configuration.

To determine the most desirable type of connection let us assume the frequency range of the amplifier will be low compared to the frequency of alpha cut-off. The circuit is arranged so that the output current of the stage passes entirely into the final stage. Then the current in the input is

$$I_{in} = \frac{E_g}{R_g + R_{in}}$$

where E_g = generator voltage

R_g = generator impedance

R_{in} = input impedance of final amplifier

The current in the output circuit is

$$I_o = \left(\frac{E_g}{R_g + R_{in}}\right) Ai$$

where Ai is the current gain of the stage

The power delivered to the final amplifier is then

$$\frac{R_{in} \quad (E_g \quad A_i)}{(R_g + R_{in})}$$

Since the power transfer from a generator to a matched load is $\frac{E_g}{4 R_g}$

the power gain is

$$P_G = \frac{4 \quad R_{in} R_g \quad A_i}{(R_g + R_{in})}$$

Let $$\frac{R_g \quad A_i}{(R_g + R_{in})} = K$$

The variation of K vs R_g for the grounded base, grounded emitter, and grounded collector configurations is shown in figure 9. [14] From this figure it can be seen that if R_g is small it is desirable to use the grounded base or grounded emitter. If R_g is intermediate it is desirable to use the grounded emitter. If R_g is large, the grounded emitter or grounded collector is most desirable.

R. L. Riddle in an article on two-stage transistor amplifiers, [8] analyzes the nine possible configurations of a two stage amplifier. Figure 10 presents a summary of these results. In the gain equations R is the load resistance of the last stage and R_{in} is the input resistance to the first stage. The assumption is made that the transistors have the same alpha and that a ≈ alpha. The equations also neglect interstage losses.

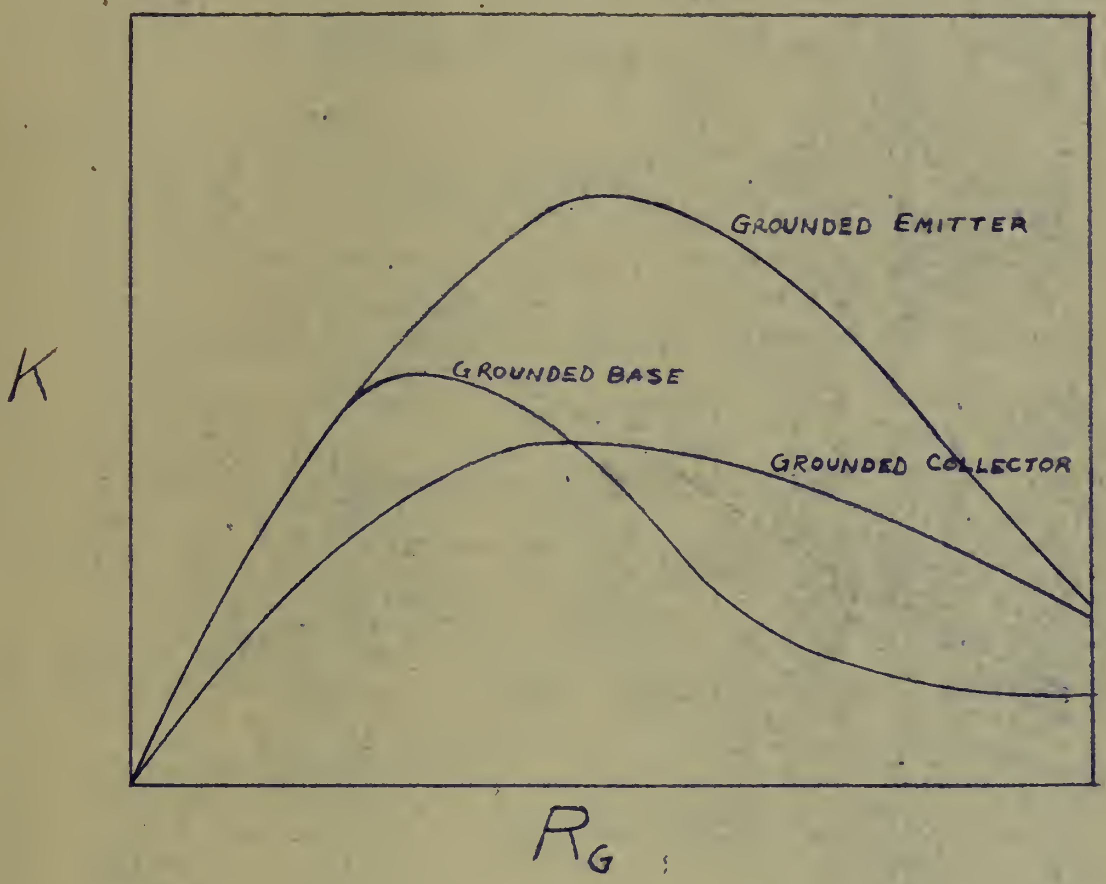


FIGURE 9

CIRCUIT	GAIN	RELATIVE INPUT IMPEDANCE	RELATIVE OUTPUT IMPEDANCE	GAIN IN DB
GE TO GE	$\frac{R_L}{R_{IN}}\left(\frac{a}{1-a}\right)^4$	MED	MED	67 DB
GE TO GC	$\frac{R_L}{R_{IN}}\left(\frac{a^2}{1-a}\right)^4$	MED	LOW	51 DB
GE TO GB	$\frac{R_L}{R_{IN}}\frac{(a^4)}{(1-a)^2}$	MED	HIGH	35 DB
GC TO GC	$\frac{R_L}{R_{IN}}\left(\frac{1}{1-a}\right)^4$	HIGH	LOW	25 DB
GC TO GE	$\frac{R_L}{R_{IN}}\frac{a^2}{(1-a)^4}$	HIGH	MED	50 DB
GC TO GB	$\frac{R_L}{R_{IN}}\left(\frac{a}{1-a}\right)^2$	HIGH	HIGH	30 DB
GB TO GB	$\frac{R_L}{R_{IN}}a^2$	LOW	HIGH	25 DB
GB TO GE	$\frac{R_L}{R_{IN}}\frac{a^4}{(1-a)^2}$	LOW	MED	52 DB
GB TO GC	$\frac{R_L}{R_{IN}}\left(\frac{a}{1-a}\right)^2$	LOW	LOW	52 DB

THEORETICAL DATA FOR TWO STAGE TRANSISTOR AMPLIFIERS

FIGURE 10

Since the final stage of this amplifier is a grounded base stage it characteristically presents a low impedance to the driver. To provide a close impedance match without the use of a coupling transformer a grounded collector stage might be used. The gain of this type of configuration, however, is limited to approximately $\frac{1}{1 - a}$. Having limited the gain in the final stage in order to keep down distortion, it would be impractical to employ such a low gain configuration as the driver stage of the amplifier.

Let us next consider the grounded base as a possible choice. This circuit arrangement presents a high output impedance to the final stage and therefore requires transformer coupling if the desired gain is to be derived. The advantages of this configuration are relatively high gain, low distortion, and high stability.

Like the grounded base stage a grounded emitter driver stage would necessitate the use of transformer coupling to the output stage. The output impedance of this type of circuit not being as great, normally, as that of the grounded base would therefore present an easier matching problem and make the transformer design requirements less complex.

With respect to power gain, the grounded emitter configuration can provide $\frac{1}{1 - a}$ times the power gain of the grounded base circuit. Though the gain is increased by this factor, it can be seen that the stability is at the same time decreased by the same amount. Hence, change in transistors of different alpha's could produce considerable variations in gain of the amplifier.

2. Distortion.

Although the problem of distortion in the driver stage is decreased due to the reduction in the required power output, it is still a major requirement in the circuit design, and care must be taken to keep it to a minimum. Appendix I shows the output characteristics of the Texas Instrument germanium grown junction transistor Tl - 200. The operating point of $V_c = 10$ v, $I_c = 2.5$ ma is selected to insure that the range of operation is the most linear portion of the characteristics that exists with this type of configuration. Although the grounded base characteristics are essentially parallel and evenly spaced, those of the grounded emitter change slope and become crowded at higher values of collector current. As in the final amplifier, it can be expected that an optimum load will exist for this stage. Figure 11 shows a grounded emitter stage with a variable load and the distortion produced for various values of R .

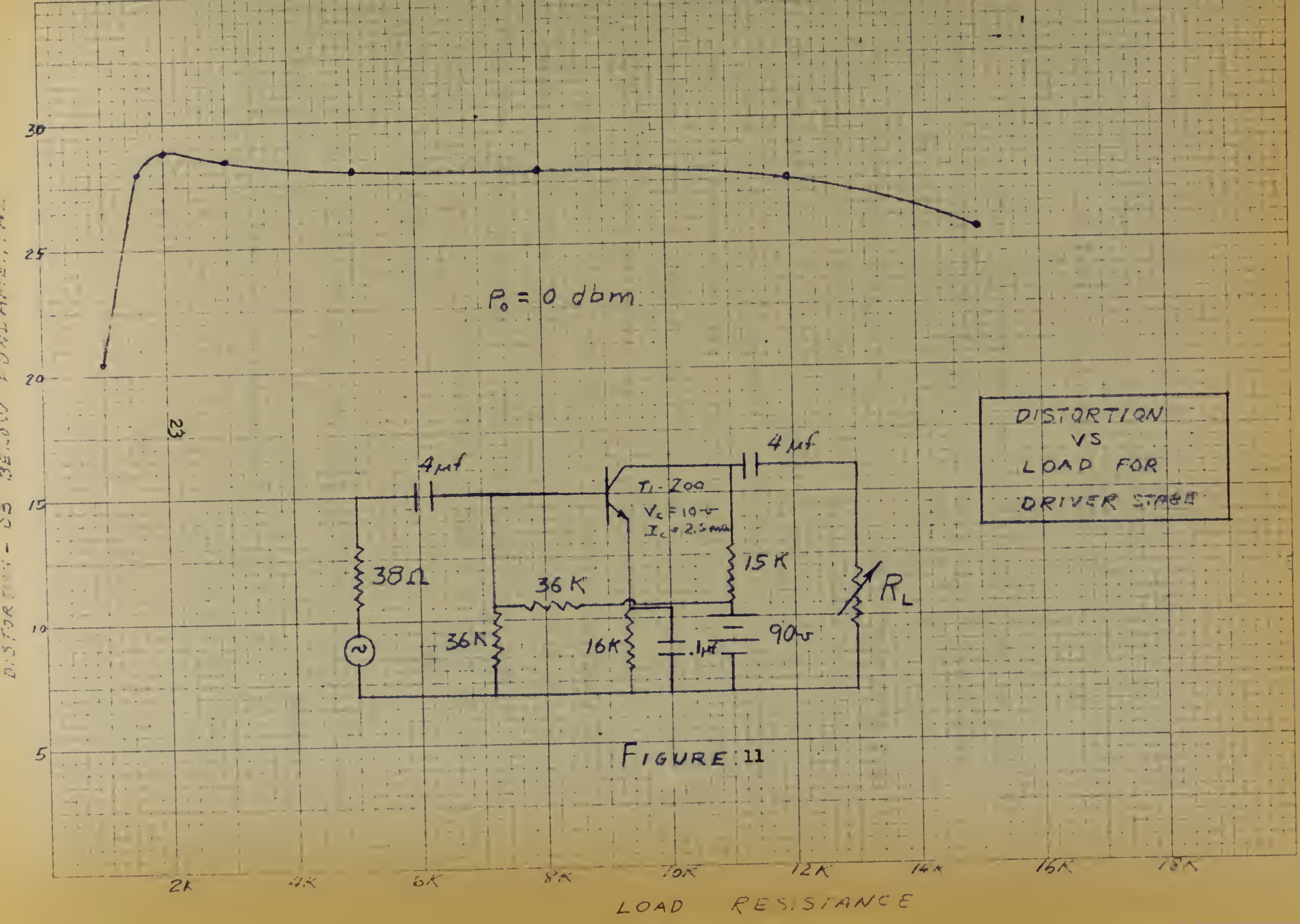
From the above data a coupling transformer with an impedance ratio of 2K:20 ohms was selected to couple the driver stage to the final amplifier.

The current excursion of I_e in the final amplifier is seen in figure 1 to be (10.2 - .1) ma = 10.1 ma

$$20 \times 10.1 \times 10^{-3} = .202 \text{ v}$$

The driver amplifier output circuit would, therefore, provide a voltage excursion of $.202 \left(\frac{N_1}{N_2}\right)$ or $.202 \times 10 = 2.02$ v. and a current excursion of 10.1 ma $\left(\frac{N_2}{N_1}\right)$ or $10.1 \times .1 = 1.01$ ma.

The output impedance of the driver stage is in the order of 15 K.



DISTORTION
VS
LOAD FOR
DRIVER STAGE

FIGURE 11

3. Source Impedance.

Having determined the output circuit of the driver stage which will produce the minimum distortion, the next step is to examine the non-linearities of the input circuit and the effects produced by the source impedance.

Figure 12 shows the collector current of a grounded emitter stage of a typical transistor as a function of the base current and of generator voltage, for zero impedance, 600 ohms, and 1200 ohms [11]. It can be seen that the relationship between input and output currents is no longer linear. This is due to the uneven spacing of the collector characteristics. It is possible to achieve a certain degree of compensation at the low current end since the I_e versus I_b versus V_b curves bend in opposite directions. From this it can be noted that in a grounded emitter amplifier it is possible to find a generator impedance which provides the best compromise between non-linearities at one end and at the other end.

By using the circuit shown in figure 13, and varying the source impedance, the optimum value for this stage was found to be approximately 100 ohms. The data, distortion versus source impedance, is also plotted in figure 13. Figure 14 shows the total distortion in the first two stages versus frequency.

4. Gain.

Of the three possible transistor configurations that of the grounded emitter is capable of producing the greatest power gain. The approximate formula for power gain at low frequencies is:

$$P_G = \frac{a^2}{(1-a)} \frac{r_l}{r_l + r_b (1-a)}$$

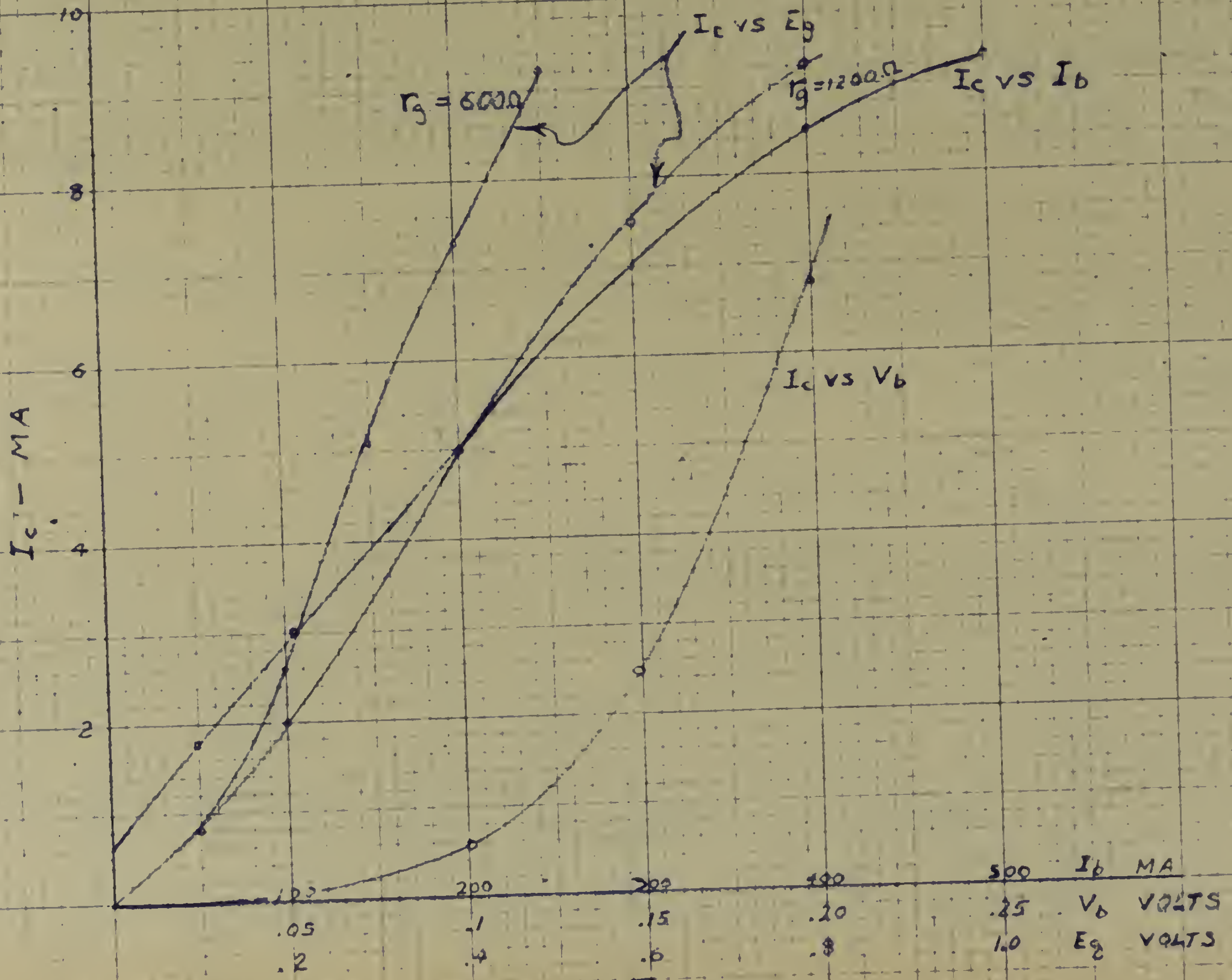

I_c vs E_g
$r_g = 600\Omega$
$r_g = 1200\Omega$
I_c vs I_b
I_c vs V_b
I_c – MA
10
8
6
4
2
100
200
300
400
500
I_b MA
.05
.1
.15
.20
.25
V_b VOLTS
.2
.4
.6
.8
1.0
E_g VOLTS

FIGURE 12

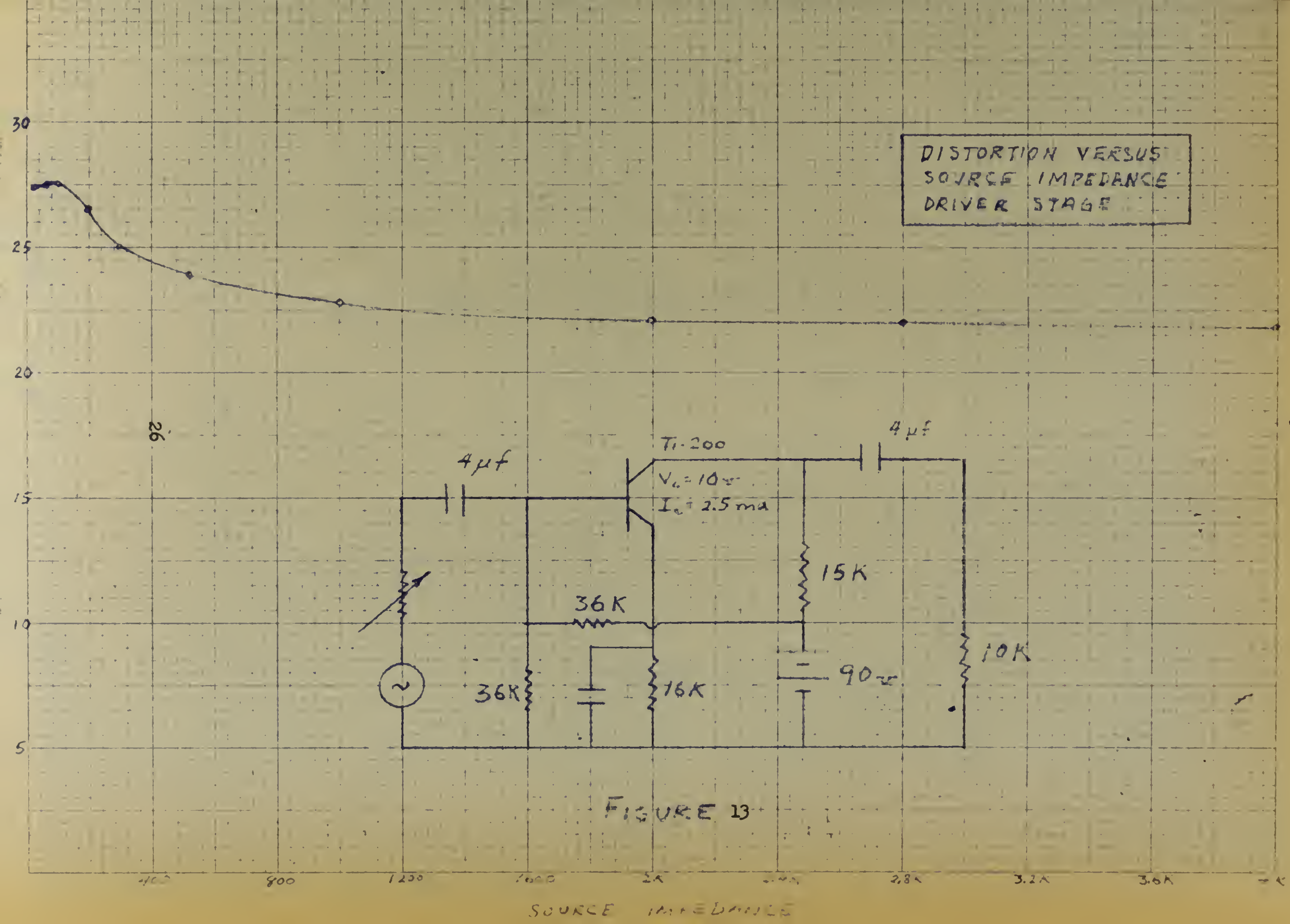

DISTORTION VERSUS
SOURCE IMPEDANCE
DRIVER STAGE
30
25
20
15
10
5
400
800
1200
1600
2K
2.4K
2.8K
3.2K
3.6K
SOURCE IMPEDANCE
4μf
Ti-200
$V_c = 10v$
$I_c = 2.5$ ma
4μf
15K
36K
36K
16K
90v
10K

FIGURE 13

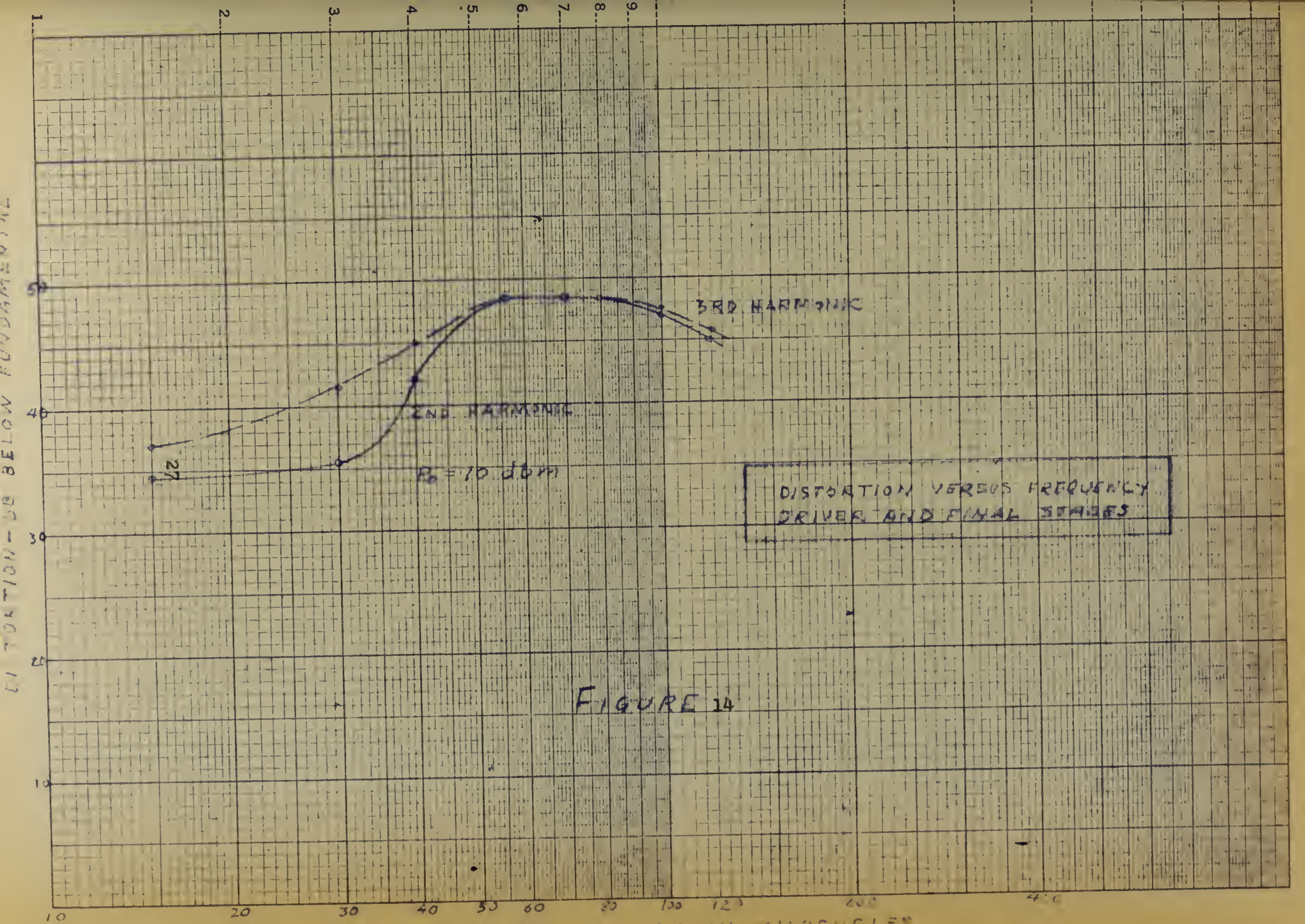

DISTORTION VERSUS FREQUENCY
DRIVER AND FINAL SERIES
3RD HARMONIC
2ND HARMONIC
$P_o = 10$ dbm
27
DISTORTION - DB BELOW FUNDAMENTAL
50
40
30
20
10
1
2
3
4
5
6
7
8
9
10
20
30
40
50
60
80
100
120
200
400

FIGURE 14

This can also be expressed as:

$$P_G = \frac{A_i \quad r_e}{r_i}$$

for a grounded emitter amplifier $A_i = \frac{a}{1-a}$

Therefore $P_G =$ is proportional to $\left(\frac{a}{1-a}\right)^2$

At low frequencies transistors of high alpha are desirable for highest gain. In the grounded emitter case the use of high alpha transistors introduces the problem of a low b cutoff frequency, since $f_{bco} = f_{aco}$ (1-a). At higher frequencies therefore, it may become necessary to use relatively low alpha transistors to avoid operation in the region of b cut-off.

For the driver stage of the amplifier being designed a transistor with an alpha of .93 and alpha cut-off of 1 MC was used. Then $f_{bco} = 10^6$ $(1-.93) = 70$ KCS.

Figure 15 shows the frequency response of the driver and final stages of the amplifier. Comparing this curve to that of figure 7 it can be seen that the grounded emitter stage tends to rapidly decrease the gain of the amplifier as the b cut-off frequency is approached.

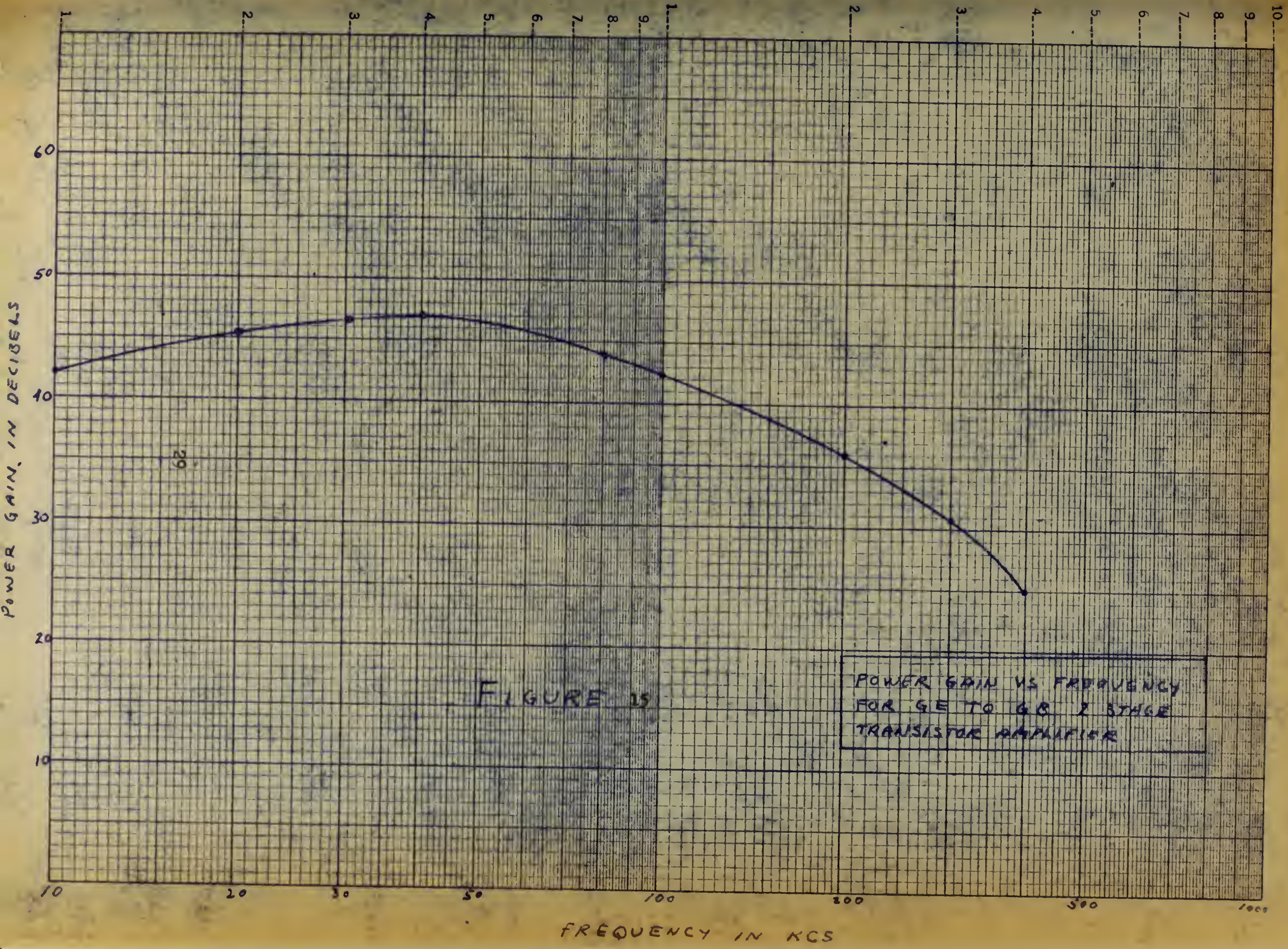


FIGURE 15

POWER GAIN VS FREQUENCY FOR GE TO 66 2 STAGE TRANSISTOR AMPLIFIER

CHAPTER IV

THE INPUT STAGE

1. General.

The primary purpose of the input stage of a 3 stage transistor power amplifier is to provide the maximum available gain. The input signal is normally of such low value that the problem of distortion in this stage becomes insignificant when compared to the distortion produced in the final and driver stages. In addition to providing high gain it is desirable to use a circuit configuration such that the output impedance of the stage will not produce an excessive mismatch with the input impedance of the second stage. Referring to figures 9 and 10 it can be seen that the grounded emitter configuration has the most desirable characteristics for this stage.

2. Distortion.

Though the distortion in this stage presents no particular problem, it was shown that the distortion in the driver stage depended considerably on the output impedance of the first stage. It becomes necessary, therefore, for the input stage to present a source impedance to the driver that produces the lowest distortion.

In the case where the driver is a grounded emitter stage it was shown that an optimum value of source impedance could be found. For this particular design problem this value was found to be approximately 100 ohms.

Once again, therefore, it becomes necessary to deviate from the normal approach to selecting the circuit configuration of the stage and modify the considerations to allow for the proper source impedance demanded by the distortion specifications.

3. Design Considerations.

Three possible circuit configurations present themselves. Namely: use of a grounded collector circuit with its inherently low output impedance, use of a grounded emitter circuit shunted with a low impedance load, or use of a grounded emitter circuit with transformer coupling between stages.

The first possibility was examined and found to produce insufficient gain. In addition, since the source impedance to the driver stage is the output impedance of the grounded collector stage it would vary from transistor to transistor. This would require a selection process of transistors to insure that the output impedance is of the proper value.

The next two possibilities were examined in order and the results are shown plotted in figure 16. These results indicate that a large loss in gain is incurred by the use of a low shunt load. To compensate for this loss would require the use of an interstage transformer.

Since the required gain of the amplifier is only 40 db, the grounded emitter configuration with a low shunt load and without transformer coupling provides the required gain with sufficient excess gain to allow for the use of negative feedback.

In addition to providing the required gain this circuit provides a source impedance to the driver which is independent of the output

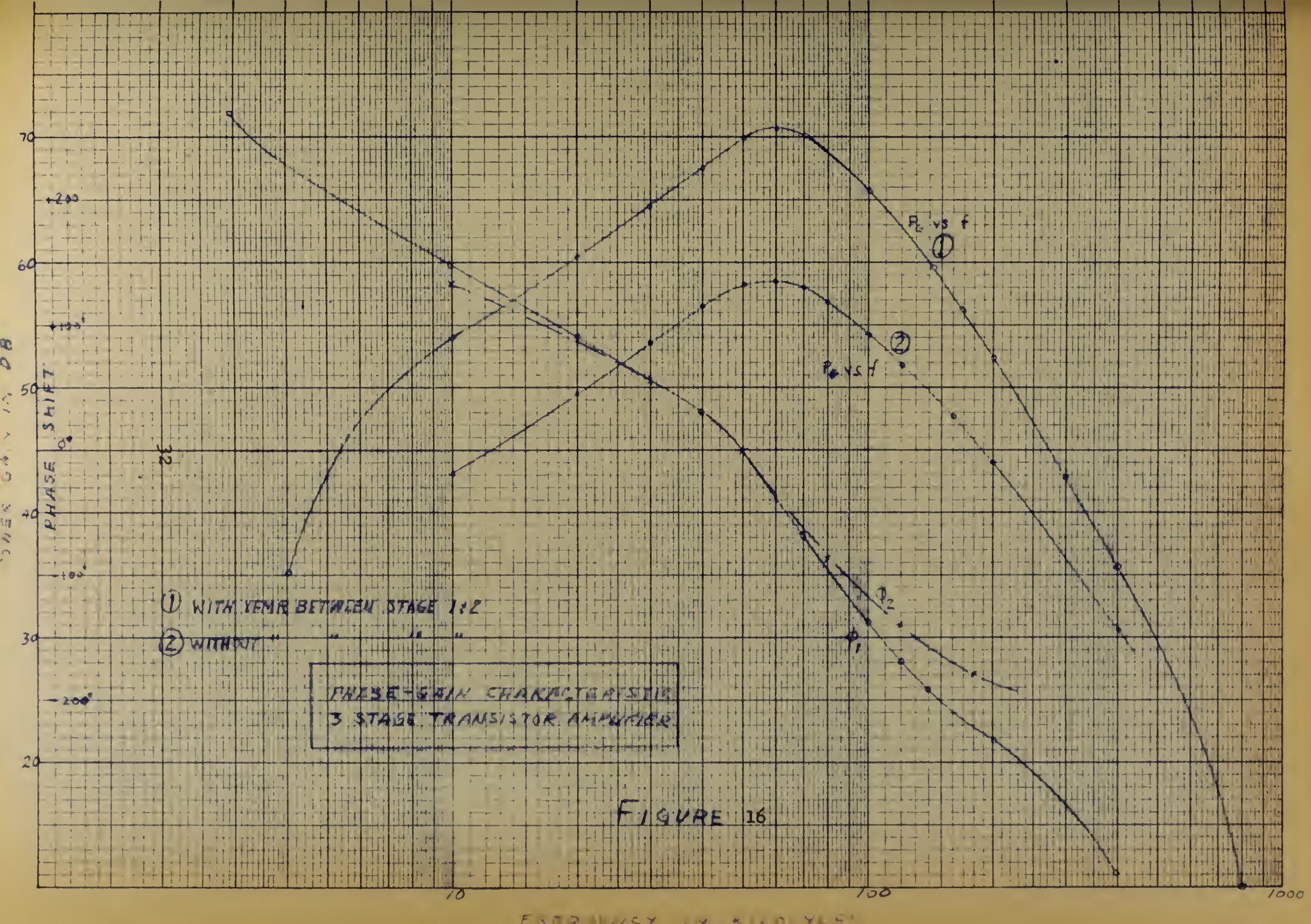

70
60
50
40
30
20
+200
+100°
0°
-100°
-200°
POWER GAIN IN DB
PHASE SHIFT
10
100
1000
FREQUENCY IN KILOCYCLES
P_G vs f ①
② P_G vs f
Φ_2
Φ_1
① WITH XFMR BETWEEN STAGE 1:2
② WITHOUT " " " "
PHASE-GAIN CHARACTERISTIC
3 STAGE TRANSISTOR AMPLIFIER

FIGURE 16

impedance of the first stage. Thus distortion can be kept to a minimum regardless of the interchanging of transistors in the first stage.

Figure 17 shows the 3 stage amplifier in its entirety. The dotted circuitry shown represents the feedback network employed. This network shall be discussed in a later chapter.

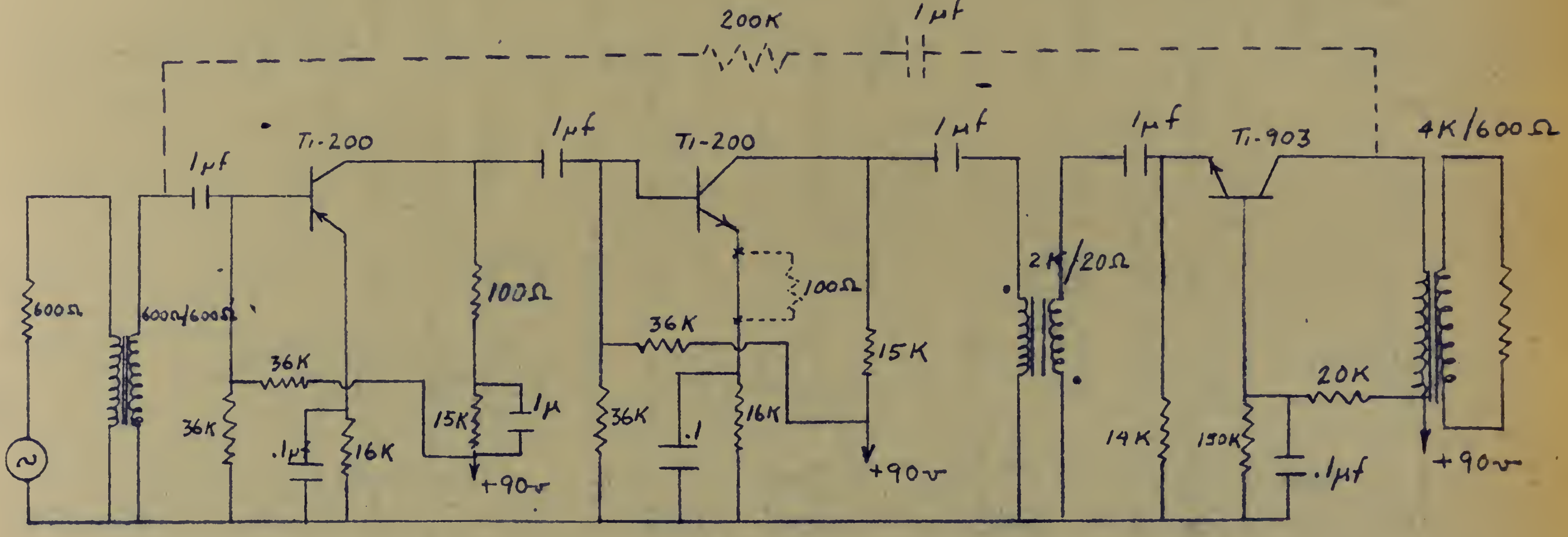

200K
1 μf
1 μf
Ti-200
1 μf
Ti-200
1 μf
1 μf
Ti-903
4K/600Ω
600Ω
600Ω/600Ω
36K
36K
.1μf
16K
100Ω
15K
1μ
+90v
36K
36K
100Ω
.1
16K
15K
+90v
2K/20Ω
14K
150K
20K
.1μf
+90v

FIGURE 17

CHAPTER V

FEEDBACK

1. General.

Since transistors have reached the stage that allow amplifiers to develop any practical value of amplification, it now becomes possible to employ methods of feedback that sacrifice gain for other more desirable qualities such as stability and linearity.

The general feedback theory for vacuum tube amplifier circuits can be used when applying feedback in transistor circuits. Some basic differences exist, however, and care must be used in its application.

In vacuum tube amplifiers it is usually possible to design a feedback loop at such an impedance level that it neither loads the output circuit appreciably, nor has any appreciable transmission in the forward direction. This is not necessarily true for transistor amplifiers, furthermore, in applying feedback around a transistor stage it is possible to reduce the power available to the load. This is usually not the case in vacuum tube amplifiers.

2. Effect of Feedback on Gain.

In developing the theory of feedback for transistors it is possible to consider the transistor as either a voltage actuated device or a current actuated device. Considering the latter case first, it can be shown that

$$A_i = \frac{A_0\ (1-\gamma)}{1 - A\gamma} \qquad [3]$$

where γ = percentage of output current feedback to the input of the amplifier

A_o = Current gain without feedback

A_i = Current gain with feedback

By comparing this equation with that known for vacuum tube theory it is noted that the above equation contains and additional term, namely $(1-\gamma)$. This is due to the loading effect of the γ loop on the amplifier. For amplifiers with large amounts of feedback $A_o\gamma \gg 1$ and $A_o = \frac{-(1-\gamma)}{\gamma}$.

Thus the current ratio of such an amplifier is determined by the transmission through the gamma loop.

For some applications the voltage feedback approach is more convenient to use. This method is used by Stanley Shenkerman in his article "Feedback Simplifies Transistor Amplifiers", [9] where he shows that

$$A_v = \frac{A_{vo}}{(1-BA_{vo})}$$

when $A_{vo}\,B \gg 1$ $\quad A_v = \frac{-1}{B}$

A_{vo} = voltage gain without feedback

A_v = voltage gain with feedback

B = percentage of output voltage fed back to the input of the amplifier,

These equations are recognized as the familiar feedback equations of vacuum tube theory.

In feedback networks where the gamma factor is considerably less than one, the loading effect of the current feedback loop can be neglected.

In this case, both the voltage and current feedback approaches conform to the theorems applicable to vacuum tube feedback theory.

3. Effect of Feedback on Frequency Response.

In the gain equations shown above, where $AB \gg 1$, ($A\gamma \gg 1$), the gain is dependent only on the factors beta or gamma. If the beta or gamma network is resistive then substantially constant amplification independent of frequency will be obtained. At the high or low frequencies, the amplification tends to fall off so that AB ($A\gamma$) will become small and large phase shifts become apparent. At high frequencies, this condition is aggravated by the fact that alpha becomes complex decreasing in amplitude and introducing large phase shifts. In figure 16, ϕ_1 and ϕ_2 are plots of difference in phase of output and input of the transistor amplifier of figure 17 versus frequency. These phase shifts can cause feedback which is negative at the center frequencies to become positive at the high and low frequences. This results in increase in gain at these frequencies and, if the feedback is large enough can cause the amplifier to be unstable.

In applying large amounts of feedback, it becomes necessary to use compensating networks to eliminate the peaks in gain at the high and low frequencies and insure that the amplifier does not become unstable.

A simple but effective method of increasing stability and decreasing phase shifts in a transistor amplifier employing one or more grounded emitter circuits is the use of an unbypassed resistor in the emitter branch of one or more of these stages. This produces negative current feedback causing increased gain stability at the cost of lowered overall gain.

Figure 18, shows the frequency response of the 3 stage transistor amplifier of figure 17 under the conditions: (1) no feedback, (2) shunt feedback alone, (3) series feedback resulting from a 100 ohm unbypassed resistor in the emitter leg of the center stage, and (4) a combination of the shunt and series feedback. With shunt feedback alone it can be seen that an increase in gain over the center frequency gain is experienced at the high and low frequencies, and that regeneration occurs at 115 KCS. This effect is eliminated by addition of the series feedback to the shunt feedback. The resulting curve is flat in response through the required portion of the frequency band with no regeneration occuring at the high frequencies.

Figure 17, with the feedback circuitry shown dotted, meets the requirements of gain and frequency response set down in the original specifications.

4. Effect of Feedback on Distortion.

For convenience, the voltage feedback concept shall be employed in determining the effect of negative feedback on distortion.

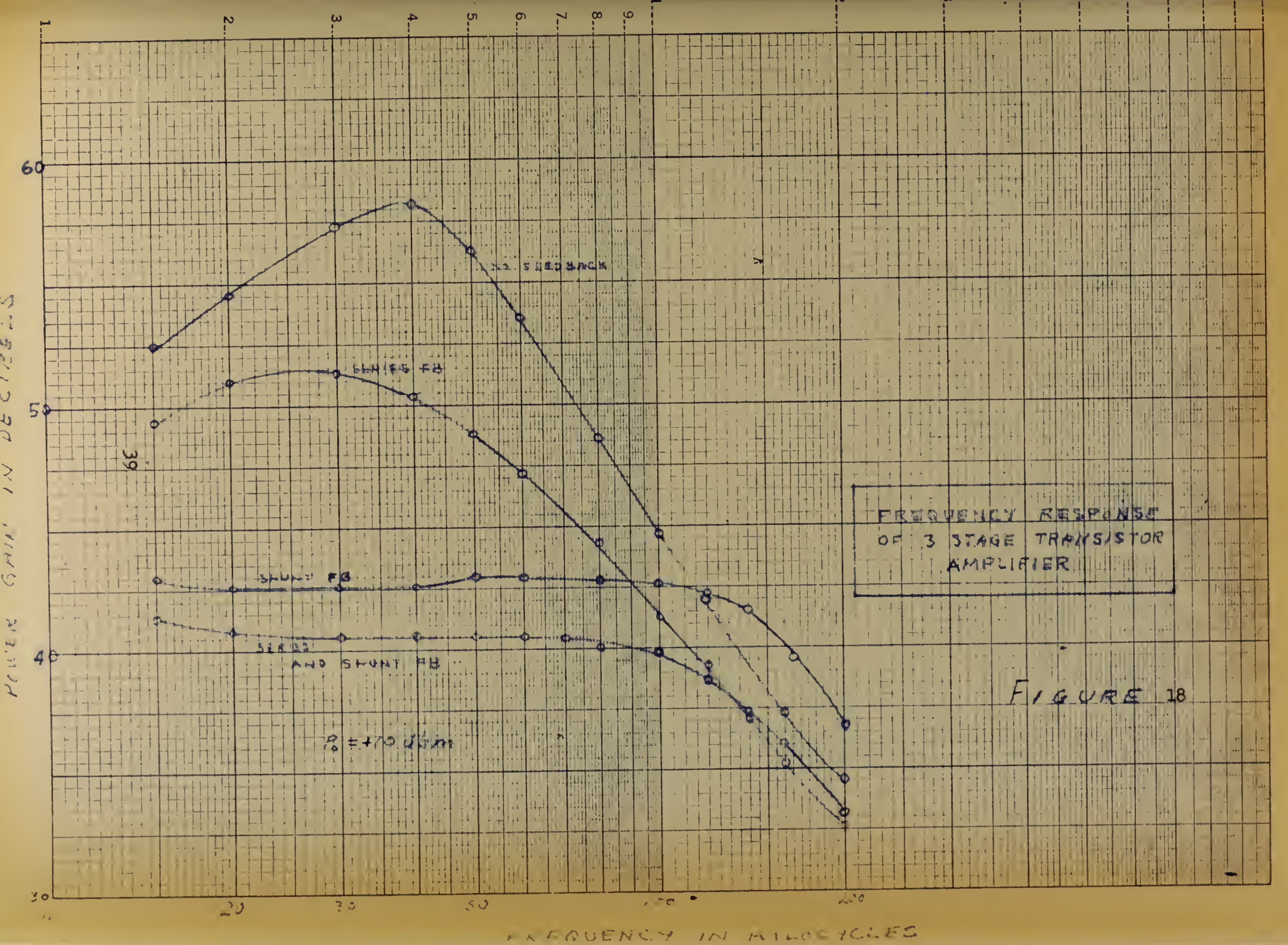
Let the input voltage be expressed as $E_1 = \sin wt$. Then the output voltage will be given by, $E_0 \sin wt + E_{02} \sin 2wt + E_{03} \sin 3 wt$.

By applying feedback, it can be shown that

$$A_2 = \frac{H_2}{1 - BA} \quad \text{and} \quad A_3 = \frac{H_3}{1-BA} \qquad [7]$$

where $A_2 =$ ratio of $\frac{E_{02}}{E_0}$ with feedback

$H_2 =$ ratio of $\frac{E_{02}}{E_0}$ without feedback



FREQUENCY RESPONSE
OF 3 STAGE TRANSISTOR
AMPLIFIER

FIGURE 18

$A_3 =$ ratio of $\frac{E_{o3}}{E_o}$ with feedback

$H_3 =$ ratio of $\frac{E_{o3}}{E_o}$ without feedback

Thus the magnitudes of all the harmonics and consequently any intermodulation products introduced by the amplifier are reduced by negative feedback in the same proportion that the gain is reduced.

These results are based on the assumptions that E_o is exactly 180 degrees out of phase with E_i , and that the amplification is the same for the harmonics as for the fundamental. By referring to figure 16, it can be seen that this is normally not the case in transistor multistage amplifiers. At lower frequencies where the harmonics have gain and phase characteristics similar to the fundamental, decreases of the order mentioned above can be expected. At higher frequencies, however, these decreases will tend to lessen, and it is even possible that the harmonic distortion will increase.

Figure 19, shows the distortion introduced in the amplifier of figure 17. A marked decrease in the effect of feedback at the higher frequencies can be seen in this figure. For the curves 2 f_1 an actual increase in distortion is experienced at the high end of the band.

The results of figure 19 meet the requirements for distortion as called for by the specifications of this amplifier.

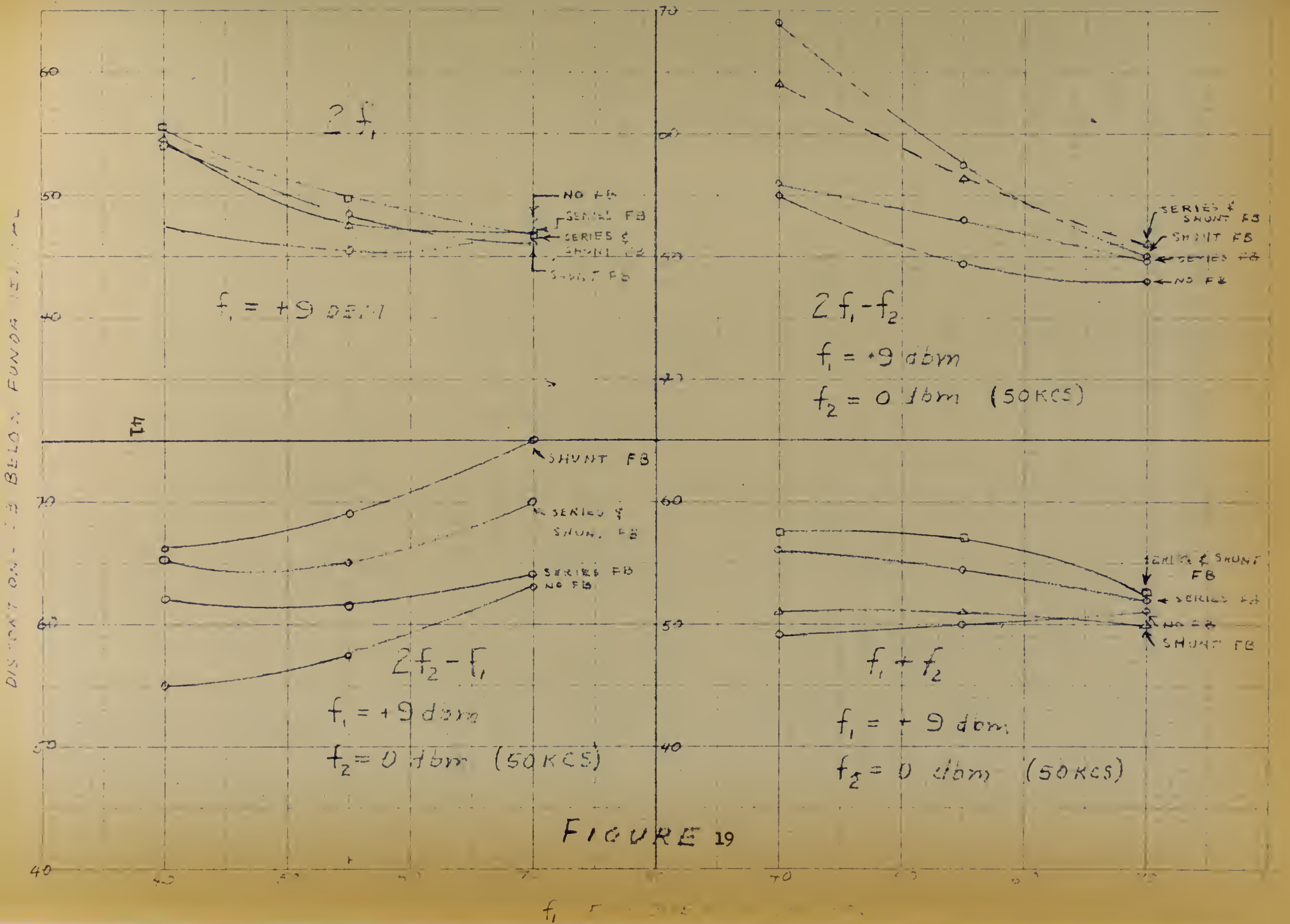

DISTORTION - DB BELOW FUNDAMENTAL
$2f_1$
$f_1 = +9$ DBM
NO FB
SERIES FB
SERIES & SHUNT FB
SHUNT FB
$2f_1 - f_2$
$f_1 = +9$ dbm
$f_2 = 0$ dbm (50KCS)
SERIES & SHUNT FB
SHUNT FB
SERIES FB
NO FB
$2f_2 - f_1$
$f_1 = +9$ dbm
$f_2 = 0$ dbm (50KCS)
SHUNT FB
SERIES & SHUNT FB
SERIES FB
NO FB
$f_1 + f_2$
$f_1 = +9$ dbm
$f_2 = 0$ dbm (50KCS)
SERIES & SHUNT FB
SERIES FB
NO FB
SHUNT FB
70
60
50
40
f_1

FIGURE 19

5. Effect of Feedback on the Input Resistance.

The effect of feedback on the input resistance depends on the method in which the feedback is applied and not whether it is voltage or current feedback. In the case of negative feedback being applied in series with the input the input resistance is increased in the same proportion that the gain is decreased. Conversely, when the feedback is applied in shunt, the input resistance is decreased. By use of both shunt and series feedback it is possible to control the value of the input resistance and to keep it constant over a wide range of frequencies. The latter characteristic is of great value in transistor amplifiers since the input impedance varies considerably at the higher frequencies.

6. Effect of Feedback on Output Resistance.

In contrast to the effect on input resistance, the type of feedback, that is current or voltage feedback, determines the effect on the output resistance. Voltage feedback decreases the output resistance and current feedback increases it. The effect of both types of feedback will be considered simultaneously by considering them applied together in a bridge type feedback circuit. From vacuum tube theory the effective plate resistance is:

$$r^{1}{}_{p} = \frac{r_p - (A_1 \mu_2 + 1)(\gamma R1)}{1 - A_1 \mu_2 B} \approx r^{1}{}_{o} \qquad [7]$$

r^{1}_{p} = plate resistance of final stage with feedback

r_p = plate resistance of final stage without feedback

μ_2 = amplification of final stage

A_1 = amplification between input and grid of final stage

r^{1}_{o} = output resistance of amplifier with feedback

Let A_2 equal the amplification of the final stage. Then

$$A_2 = \frac{\mu_2 R_1}{r_p + R_1}$$

where R_1 = load resistance.

then $\mu_2 = \frac{A_2 (r_p + R_1)}{R_1}$

and $r_o' = \frac{r_p - \left[A_1 A_2 \left(\frac{r_p}{R_1} + 1\right) + 1\right] \gamma R_1}{1 - A_1 A_2 \left(\frac{r_p}{R_L} + 1\right) \beta}$

Let $A_T = A_1 \times A_2$ = total amplification of amplifier

then $r_o' = \frac{r_p - \left[A_T \left(\frac{r_p}{R_1} + 1\right) + 1\right] \gamma R_1}{1 - A_T \left(\frac{r_p}{R_1} + 1\right) \beta}$

Considering a transistor amplifier where the distortion requirements are such as to necessitate a grounded base stage as the final stage and applying the principles of duality between transistors and vacuum tubes, the above equation may be written

$$r_o' = \frac{r_c - \left[A_T \left(\frac{r_c}{R_1} + 1\right) + 1\right] \gamma R_1}{1 - A_T \left(\frac{r_c}{R_L} + 1\right) \beta}$$

where r_c = collector resistance of transistor. By solving the above equation when $r^1_o = R_l$ and assuming $\frac{r_c}{R_L} \gg 1$, $\beta = \gamma + \frac{1}{A}$

This is the condition that must be satisfied to match the effective output resistance to the load resistance.

7. Stability.

In transistor amplifiers, it is conceivable that the power gain may vary as much as 10 decibels when the transistors of the various stages are changed. It is also quite probable that the alphas of the transistors will change with age and thus introduce changes in gain in the amplifier.

The use of negative feedback increases the stability of these amplifiers.

In the amplifier shown in figure 17 a change in gain of 8 decibels was observed by the interchanging of transistors at random from a group of transistors ranging in alpha from .92 to .975. This change was experienced when no feedback was employed. When the feedback network was connected this change in gain was decreased to 4 decibels.

This change is outside the stability required for an amplifier of this type. Therefore, it becomes necessary to limit the transistors used to a narrower range of alphas.

CHAPTER VI

STABILIZED TRANSISTOR AMPLIFIERS

1. General.

In the preceding chapters a three stage transistor amplifier consisting of a grounded emitter first stage, grounded emitter driver, and grounded base final amplifier stage was designed and the characteristics of this amplifier were described. This amplifier met the design specifications in respect to frequency response, power output, power gain, and distortion. However, as was pointed out, when different transistors were substituted into the amplifier a gain variation of 4 decibels was encountered even though 18 decibels (at center frequency) of negative feedback was applied. In an amplifier of this type it is desirable to limit this gain variation to ± .25 decibels. To meet this requirement, it becomes necessary to either change the circuit configuration or to limit the transistors used in the circuits to those having characteristics similar enough so that the small gain variation requirements are met. Since the requirements are extremely severe it becomes probable that a combination of both of these corrective measures will be required.

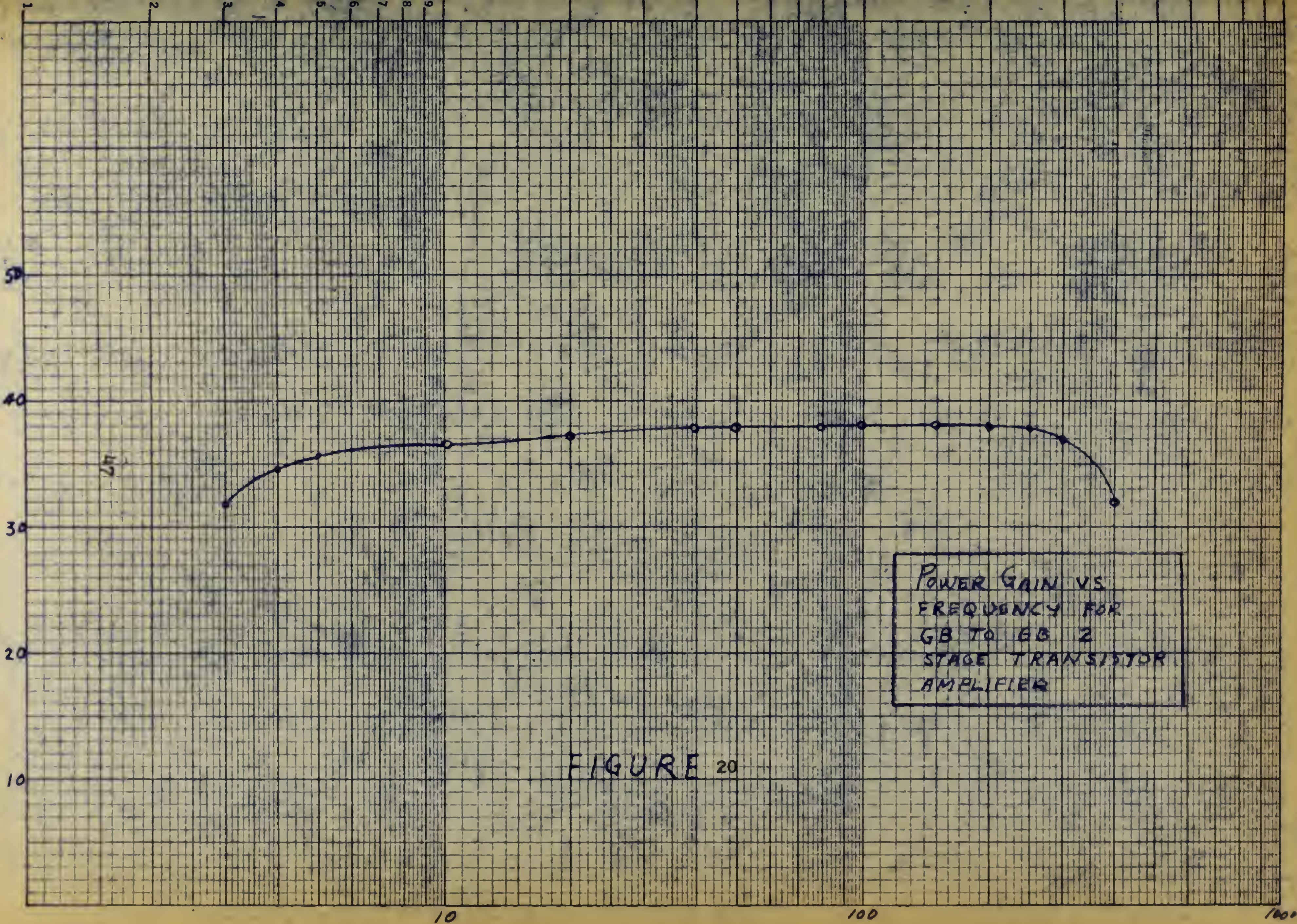
2. Circuit Design.

As was pointed out in the original design problem, the greatest amount of instability is encountered in the grounded emitter circuit. In this circuit power gain is proportional to $\frac{a^2}{(1-a)^2}$

A change in transistors from one of alpha .95 to one of alpha .90 produces a gain variation of 6 decibels. With two such stages in the amplifier a gain variation of 9 decibels is possible from the above transistor change. If the grounded emitter stages could be replaced by grounded base stages the stability problem would be greatly improved. Replacement of both stages would decrease the total power gain of the amplifier below that required by the specifications. The driver stage, however, can be replaced without an excessive loss in gain.

Figure 20 shows the frequency response of the final and driver stages. Comparing this curve with that of figure 15, it can be seen that much better frequency response is obtained by using the two grounded base stages. However, the power gain has decreased from a maximum of 47 decibels to 38 decibels. The stability of the two stages has been considerably improved. Using transistors of the same alpha ranges as those previously used, the gain variation is reduced from 6 decibels to one decibel.

As before, it is desirable to avoid the use of transformer coupling between stages 1 and 2. By using direct coupling a large mismatch exists between the output of the grounded emitter first stage and the grounded base second stage, thus introducing a considerable loss in gain. Figure 21 shows the frequency response of this type of circuit arrangement. As shown by the response curve, the maximum gain is 50.3 decibels. Hence the amount of feedback available in this circuit has been reduced to 10 decibels.



POWER GAIN VS
FREQUENCY FOR
GB TO GB 2
STAGE TRANSISTOR
AMPLIFIER

FIGURE 20

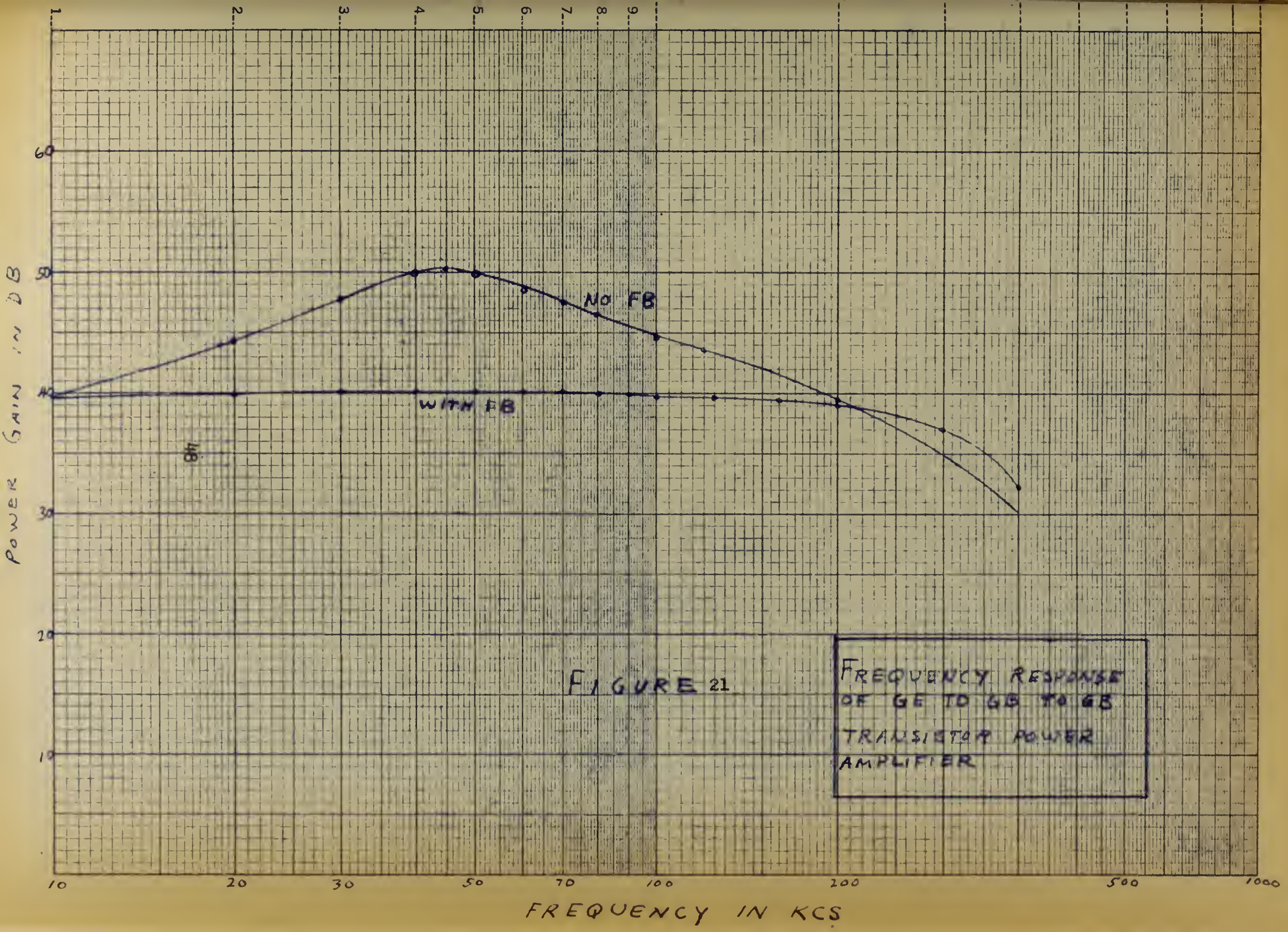


FIGURE 21

FREQUENCY RESPONSE OF GE TO GB TO GB TRANSISTOR POWER AMPLIFIER

3. Feedback.

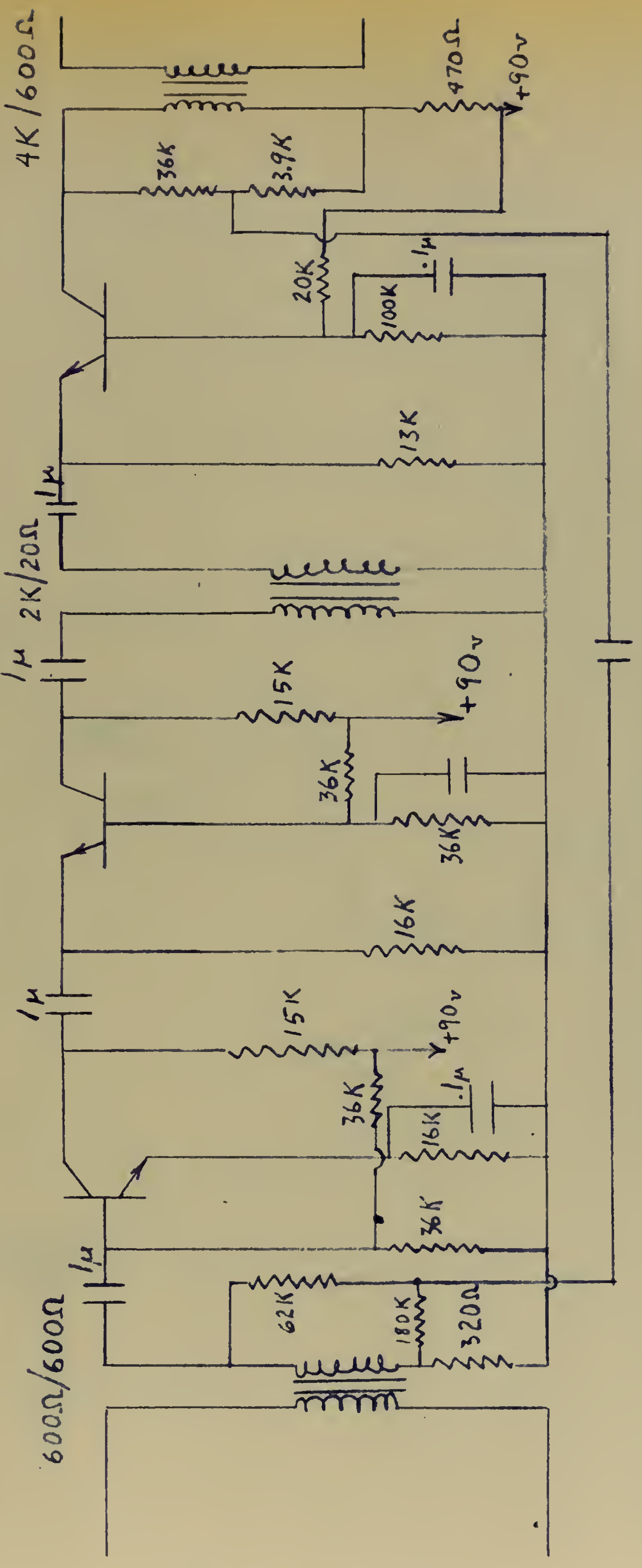
To control the output impedance of the amplifier a bridge type feedback network as analyzed in chapter 5 is used. The feedback is then applied in series and shunt with the input thus controlling the input impedance. Figure 22 shows the complete amplifier.

By using this feedback circuit configuration it was possible to control the input impedance to 600 ohms ± 5% and the output impedance to 1 K ± 10%.

4. Stability.

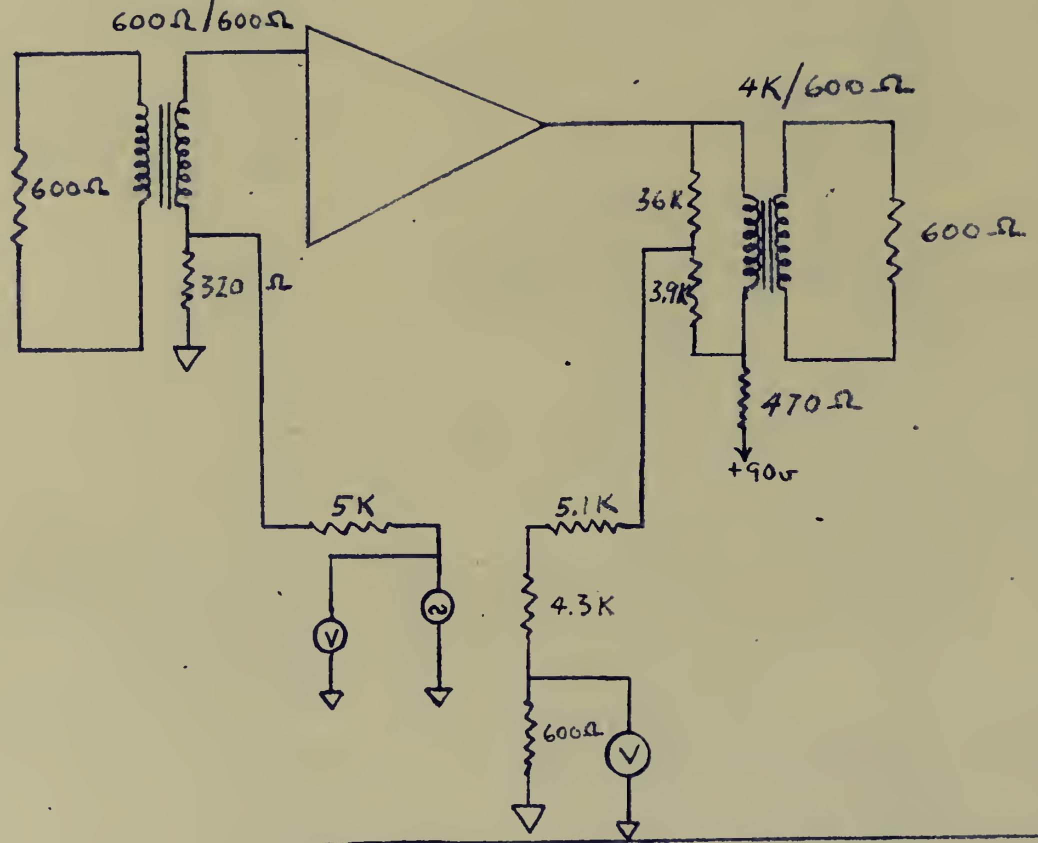
From figure 21, it is evident that the applied negative feedback becomes regenerative at the frequencies 10 kilocycles and 215 kilocycles. To determine the phase and gain margins of the amplifier, the feedback loop was broken and the circuit of figure 23 was used to determine the phase-gain characteristic. This characteristic is shown in figure 24. From this figure the phase margin was found to be + 85 degrees and the gain margin + 13 decibels indicating the amplifier is stable. This condition is further verified by the plot of AB versus phase on polar coordinates as shown in figure 25. Stability is indicated by the curve failing to encircle the point 1 + jo.

In substituting various transistors in the amplifier with alphas ranging from .90 to .955, variations in gain of 1 decibel were experienced. Though this is still above specification requirements it is a considerable improvement over the grounded emitter configuration. In order to reduce this gain variation it becomes necessary to use tran-



THREE STAGE TRANSISTOR POWER AMPLIFIER

FIGURE 22



CIRCUIT USED FOR MEASURENT OF PHASE GAIN CHARACTERISTIC OF GE TO GB TO GB TRANSISTOR AMPLIFIER.

FIGURE 23

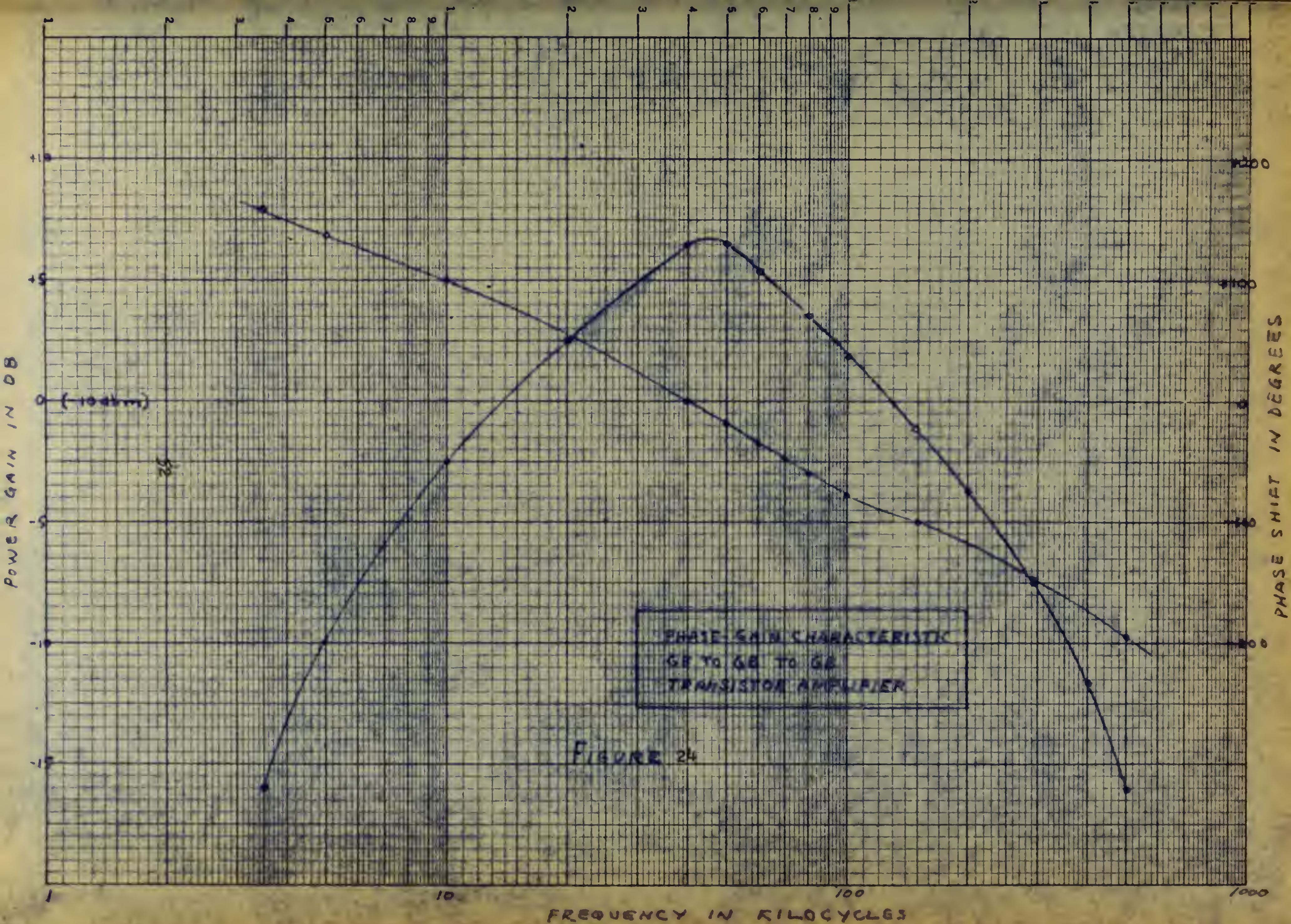

PHASE-GAIN CHARACTERISTIC
GB TO GB TO GB
TRANSISTOR AMPLIFIER
POWER GAIN IN DB
+10
+5
0 (-10dbm)
-5
-10
-15
PHASE SHIFT IN DEGREES
200
100
0
100
200
FREQUENCY IN KILOCYCLES
1
10
100
1000

FIGURE 24

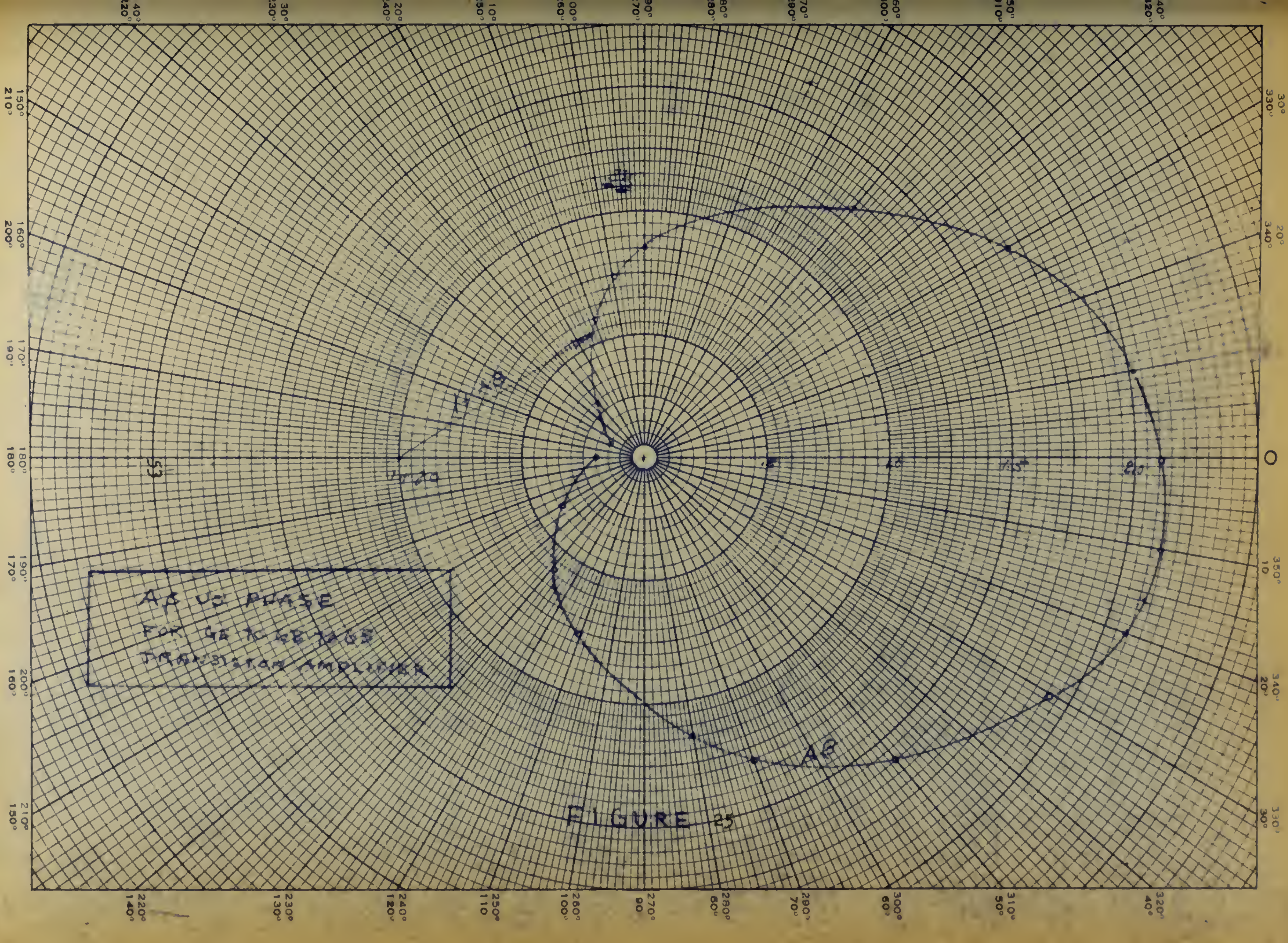


FIGURE 25

Aβ VS PHASE
FOR GE X-GE-1405
TRANSISTOR AMPLIFIER

sistors of a narrower alpha range. This range was found to be from alpha of .93 to alpha of .95. This is a rather limited range, however, this is to be expected with such stringent specification requirements.

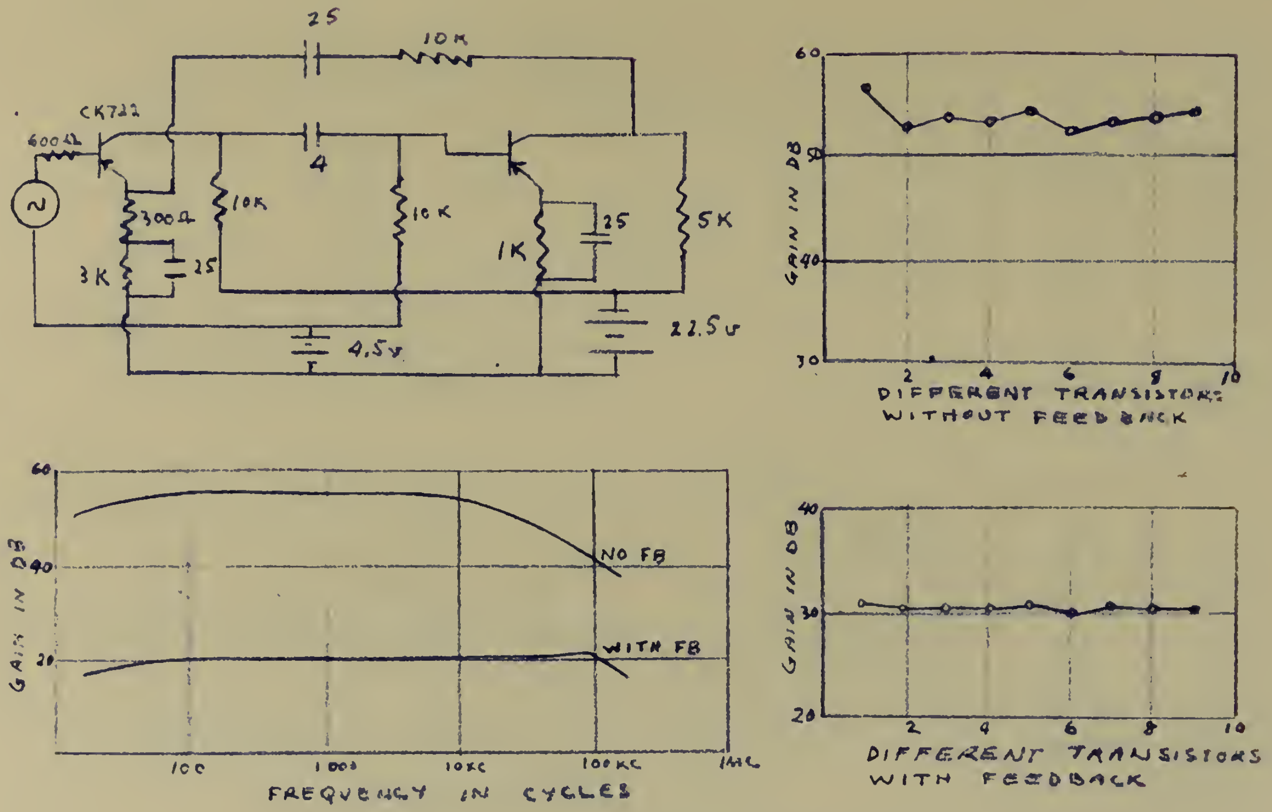
In comparison, figure 26 and 27 show two two stage transistor amplifiers with their corresponding frequency responses and variation in gain characteristics for different transistors. These amplifiers are discussed by R.L. Riddle in an article on 2-Stage transistor amplifiers [8] No information on power output or distortion is given by the author. The variations in gain, however, are given as in the order of one to two decibels. These changes are experienced even with feedback of over 30 decibels in both amplifiers.

5. Distortion.

Changing the driver stage to a grounded base stage provides the advantage of having the circuit configurations with the most linear characteristics in those portions of the amplifier in which the majority of the distortion is introduced. Consequently, the distortion without feedback is improved. Due to decrease in overall gain, however, the amount of negative feedback available is decreased. This limits the additional decrease in distortion which can be brought about by the use of negative feedback. Figure 28 shows the distortion introduced in the amplifier. These results meet the requirements as set down by the specifications.

6. Variation in Supply Voltage.

On examining the gain equations for the various transistor amplifier



GE TO GE 2 STAGE
TRANSISTOR AMPLIFIER

FIGURE 26

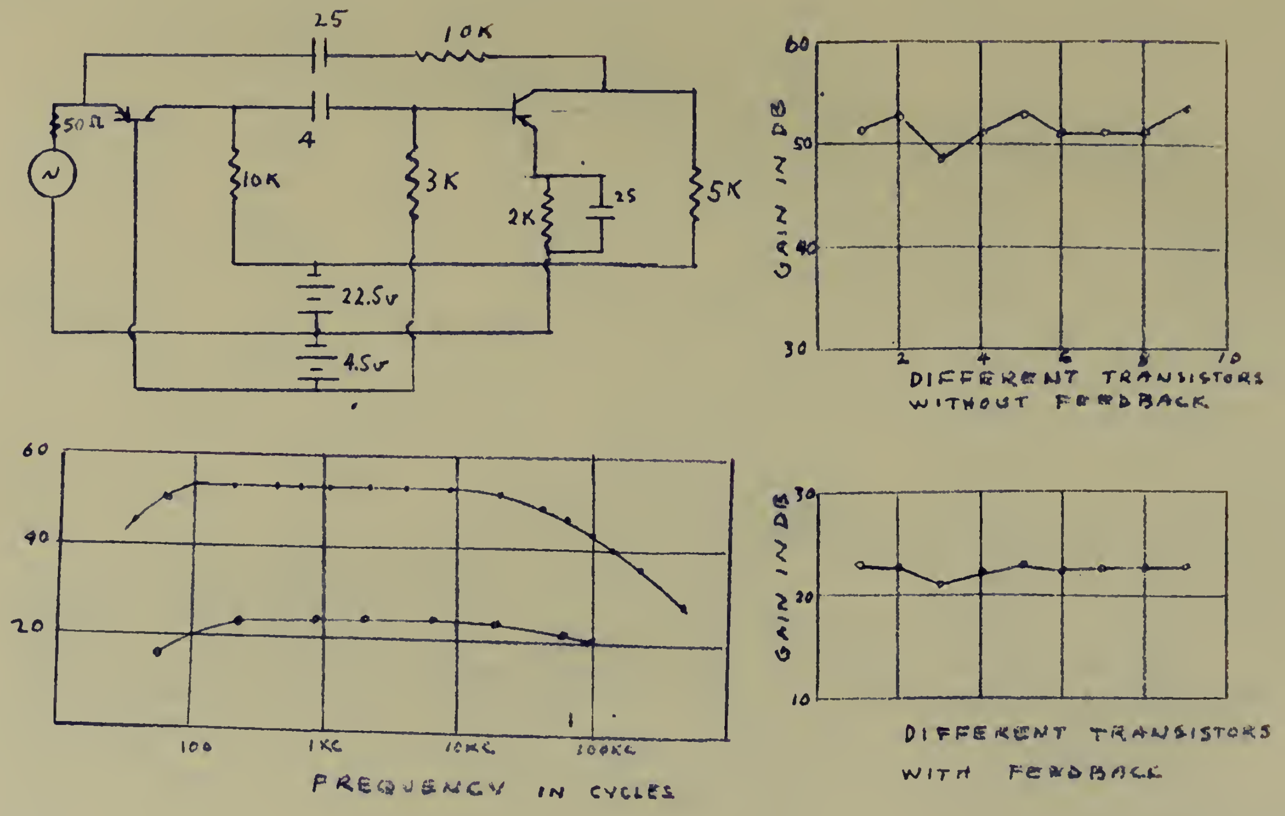


FIGURE 27

GROUNDED BASE TO
GROUNDED EMITTER
TRANSISTOR AMPLIFIER

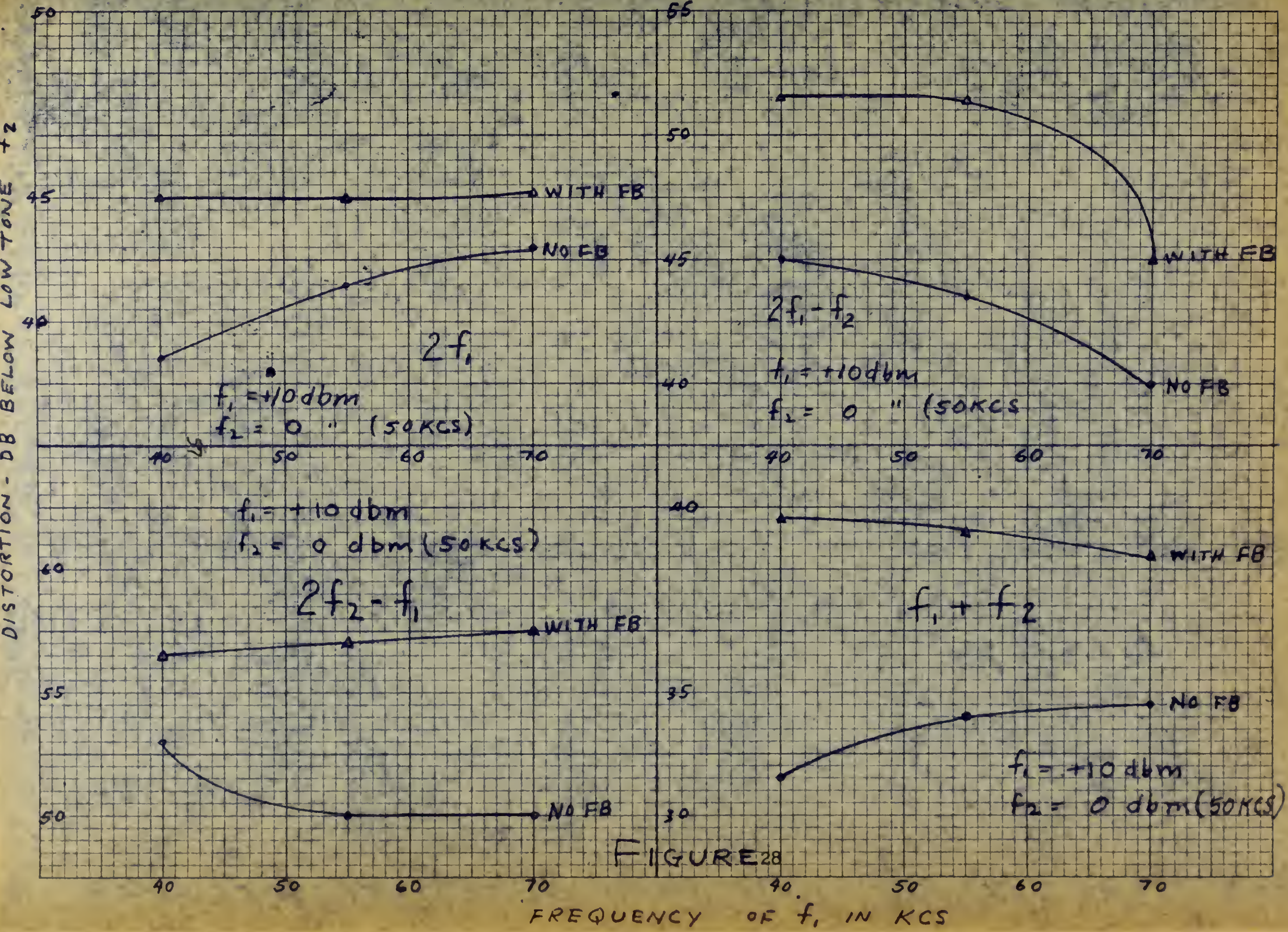

DISTORTION - DB BELOW LOW TONE f_2
FREQUENCY OF f_1 IN KCS
50
45
40
60
55
50
55
50
45
40
40
35
30
40
50
60
70
40
50
60
70
40
50
60
70
40
50
60
70
$2f_1$
f_1 =+10 dbm
f_2 = 0 " (50KCS)
WITH FB
NO FB
$2f_1 - f_2$
f_1 = +10 dbm
f_2 = 0 " (50KCS
WITH FB
NO FB
$2f_2 - f_1$
f_1 = +10 dbm
f_2 = 0 dbm (50KCS)
WITH FB
NO FB
$f_1 + f_2$
f_1 = +10 dbm
f_2 = 0 dbm (50KCS)
WITH FB
NO FB

FIGURE 28

configurations it does not seem readily apparent that the supply voltage would have any effect on the gain. It must be kept in mind, however, that the parameters of a transister experience considerable variations as the collector voltage and emitter current are changed. Consequently, by changing the supply voltage, and hence the collector voltage and emitter current, the gain can be materially effected. The stabilizing bias network tends to negate this effect.

Figure 29 shows the variation in power gain versus the supply voltage. A change in gain of less than ± .25 decibels was produced by a ± 10 per cent change in supply voltage.

A plot of the intermodulation product $2f_1 - f_2$ versus supply voltage points out the great dependency of distortion on the operating points. This is particularly true in the final stage where the input signal is large.

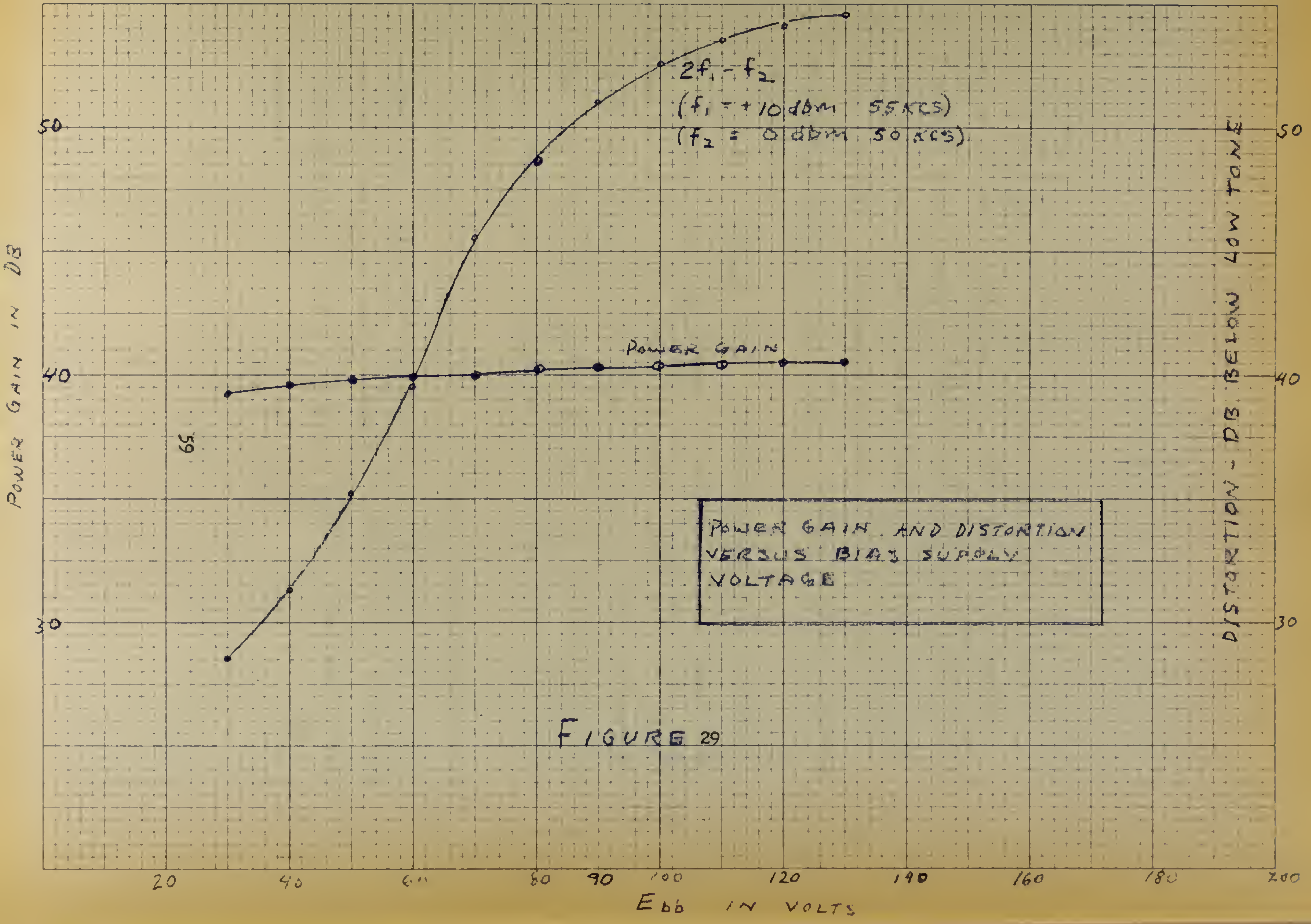

2f₁ − f₂
(f₁ = +10 dbm 55 KCS)
(f₂ = 0 dbm 50 KCS)
Power Gain
POWER GAIN AND DISTORTION VERSUS BIAS SUPPLY VOLTAGE
POWER GAIN IN DB
DISTORTION - DB. BELOW LOW TONE
Ebb IN VOLTS
50
40
30
20
40
60
80
90
100
120
140
160
180
200

FIGURE 29

CHAPTER VII

CONCLUSIONS

1. General.

In the design of low distortion power amplifiers two general methods of attack present themselves. The first, the one with which this paper deals primarily, emphasized the fact that distortion can be minimized by controlling the source impedance presented to each stage of the amplifier. The second method is to design the amplifier for maximum gain and employ large amounts of negative feedback to decrease the distortion.

The main advantage of the first method is simplicity of design. Its big disadvantage lies in the fact that to keep the distortion low large mismatches between stages are required. This decreases the gain of the amplifier materially. Since in transistor amplifiers feedback must be used for stabilization of gain and input and output impedances, a low gain amplifier limits the amount of feedback that can be used for this purpose.

The second method of design presents the converse characteristics of the first. This method provides high gain and hence ample feedback for stabilization and control purposes. However, in order to make use of this feedback it becomes necessary to employ complex phase correction networks.

Time did not permit investigation of the above method of design, and a study of the current literature on transistor power amplifiers failed to turn up any information on the subject.

2. Transistors.

Though tremendout strides have been made in transistor fabrication many problems still remain. Transistor interchangeability leaves much to be desired. It becomes necessary to employ careful selection of transistors to insure replacements in circuits that will maintain the design standards of operation. Silicon transistors ease this problem considerably, but introduce a different problem, namely that of high cost.

Looking towards the future two types of transistors show great promise. The first type, the PNIP (NPIN) junction transistor in theory indicates that the frequency range of the junction transistor triode may be extended by a factor of 10 by using a thick collector depletion layer of intrinsic semiconductor to reduce the collector capacitance and increase the collector breakdown voltage. Because of the high breakdown voltages permissible, power dissipation is much larger, thus providing greater power handling capacities as well as higher frequency operation.

The second transistor which promises to yield higher power handling capacity, greater stability, and greater range of frequency response is the field effect transistor. This transistor is a radically different form of transistor. A battery causes current to flow down the length of a semiconductor bar between contacts, one at each end of the bar, called the source and drain. These are analogous to the cathode and plate of

a vacuum tube. In the center of the bar a fused junction controls the current flowing along the bar by the electric fields which it sets up. This junction called a gate functions somewhat as the grid of a triode vacuum tube.

Though the potentialities of this transistor have thus far not been exploited to the fullest, it is considered by many to offer the best hope for a high frequency power transistor.

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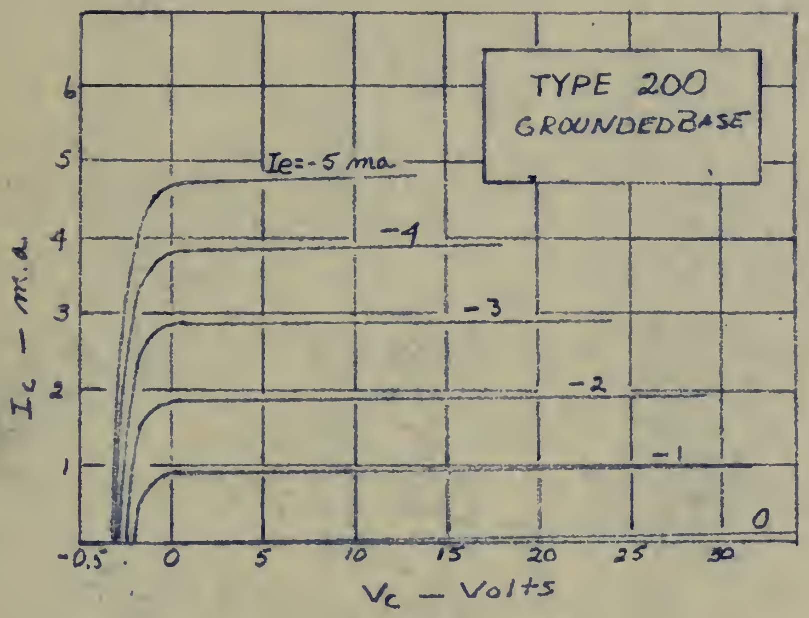
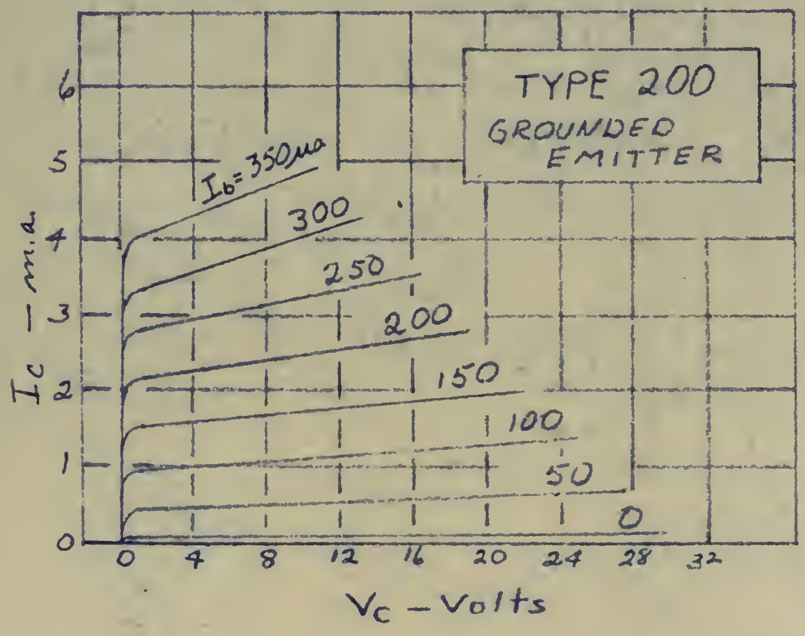
APPENDIX I

OUTPUT CHARACTERISTIC CURVES





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